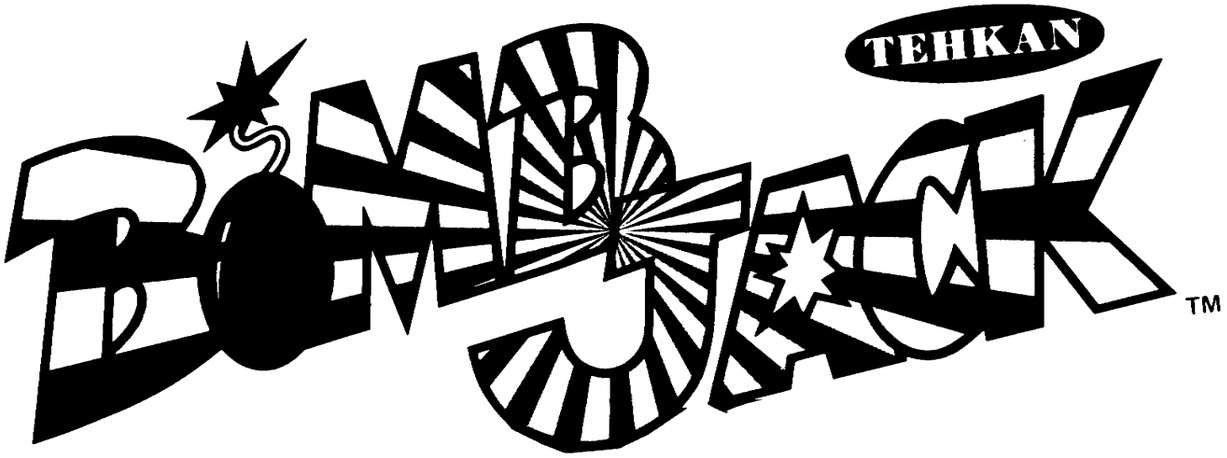

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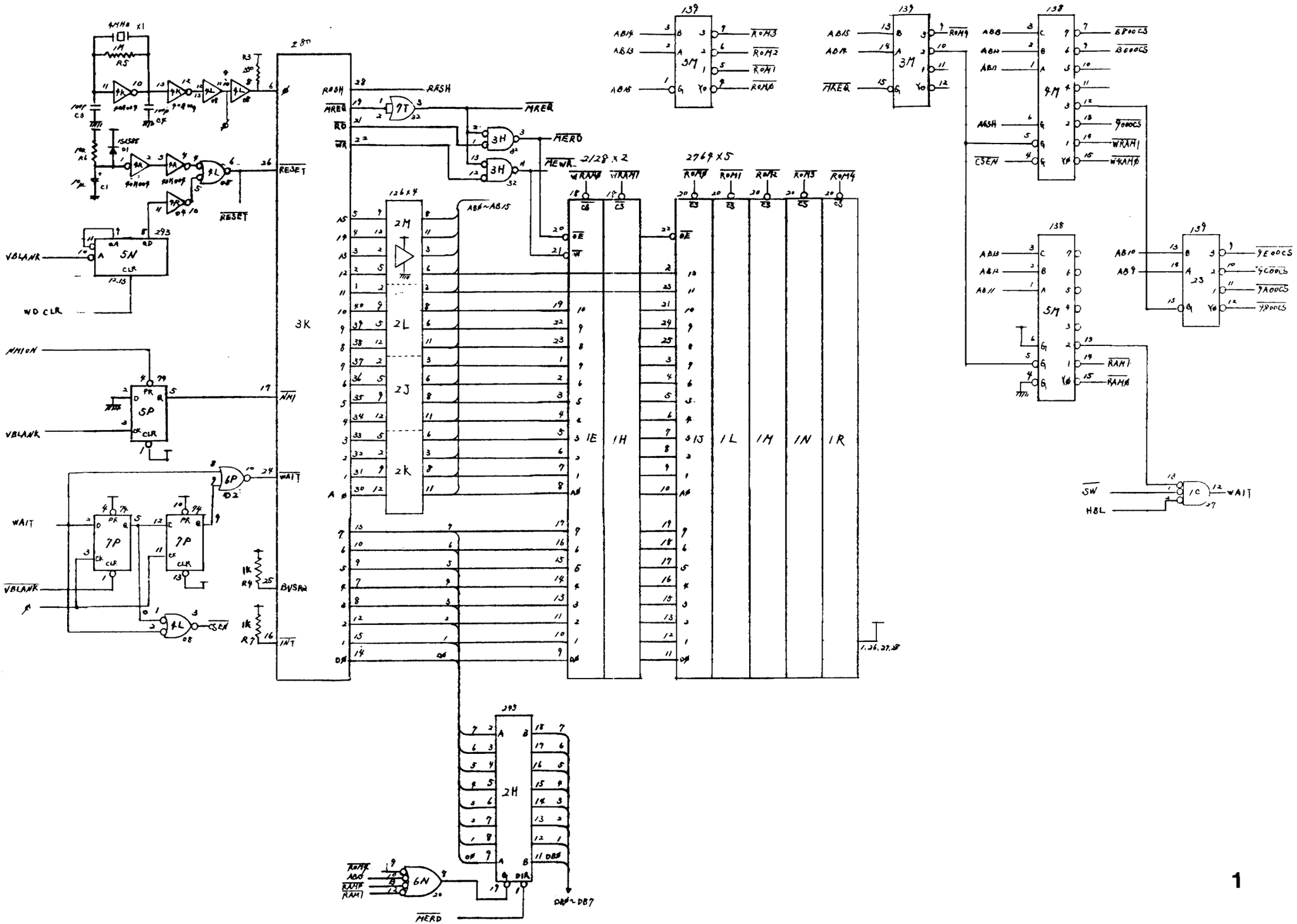
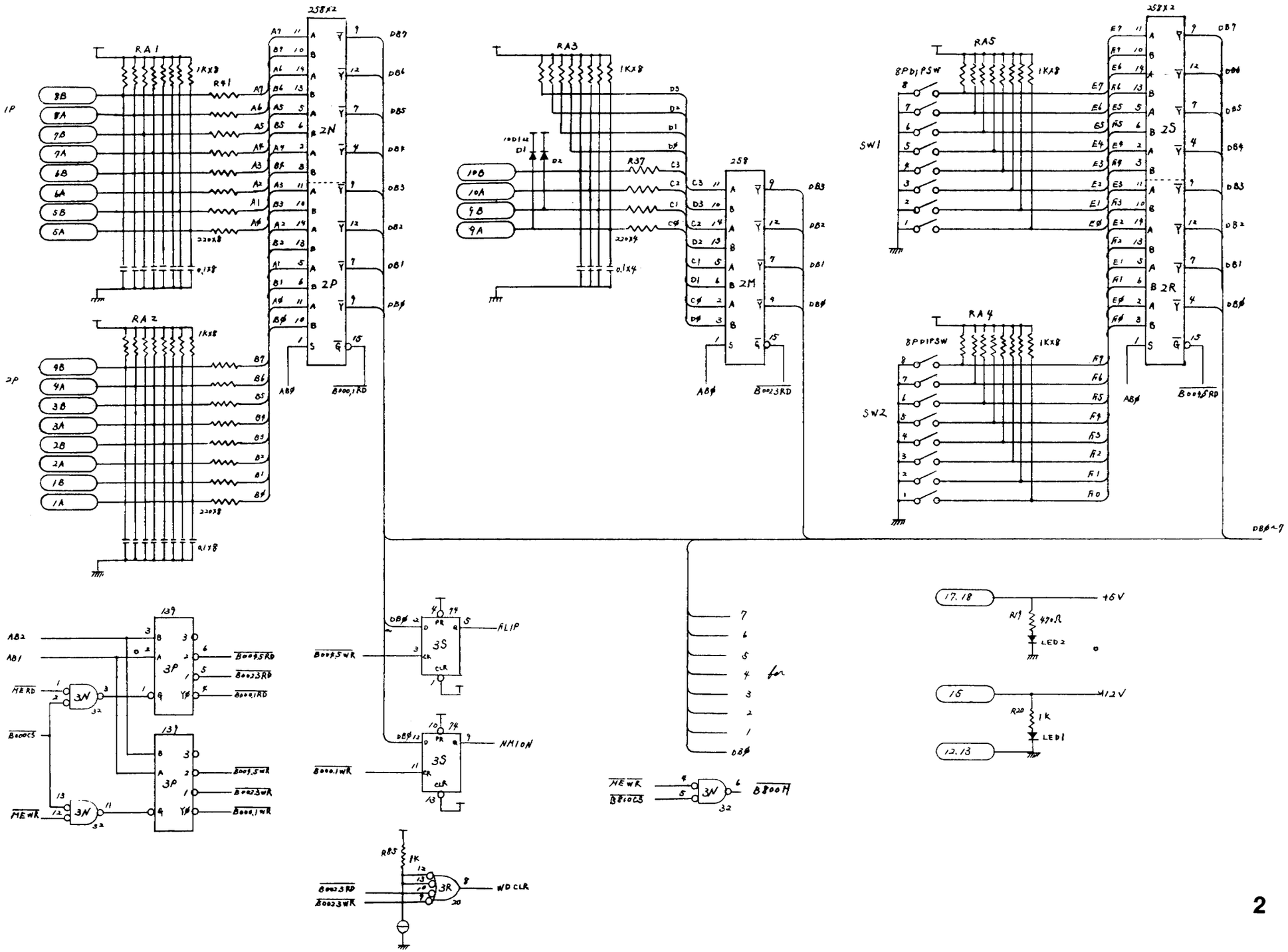
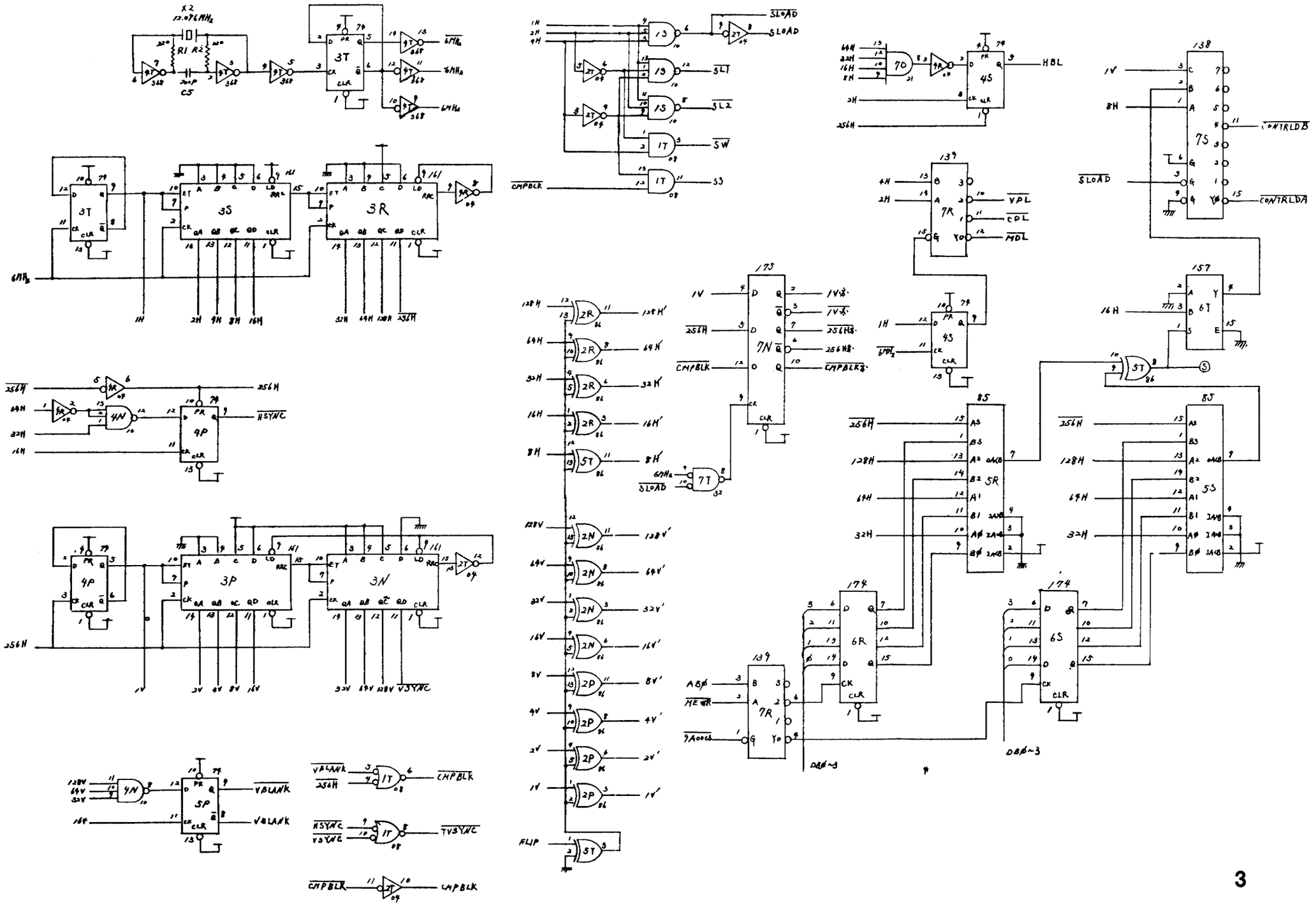
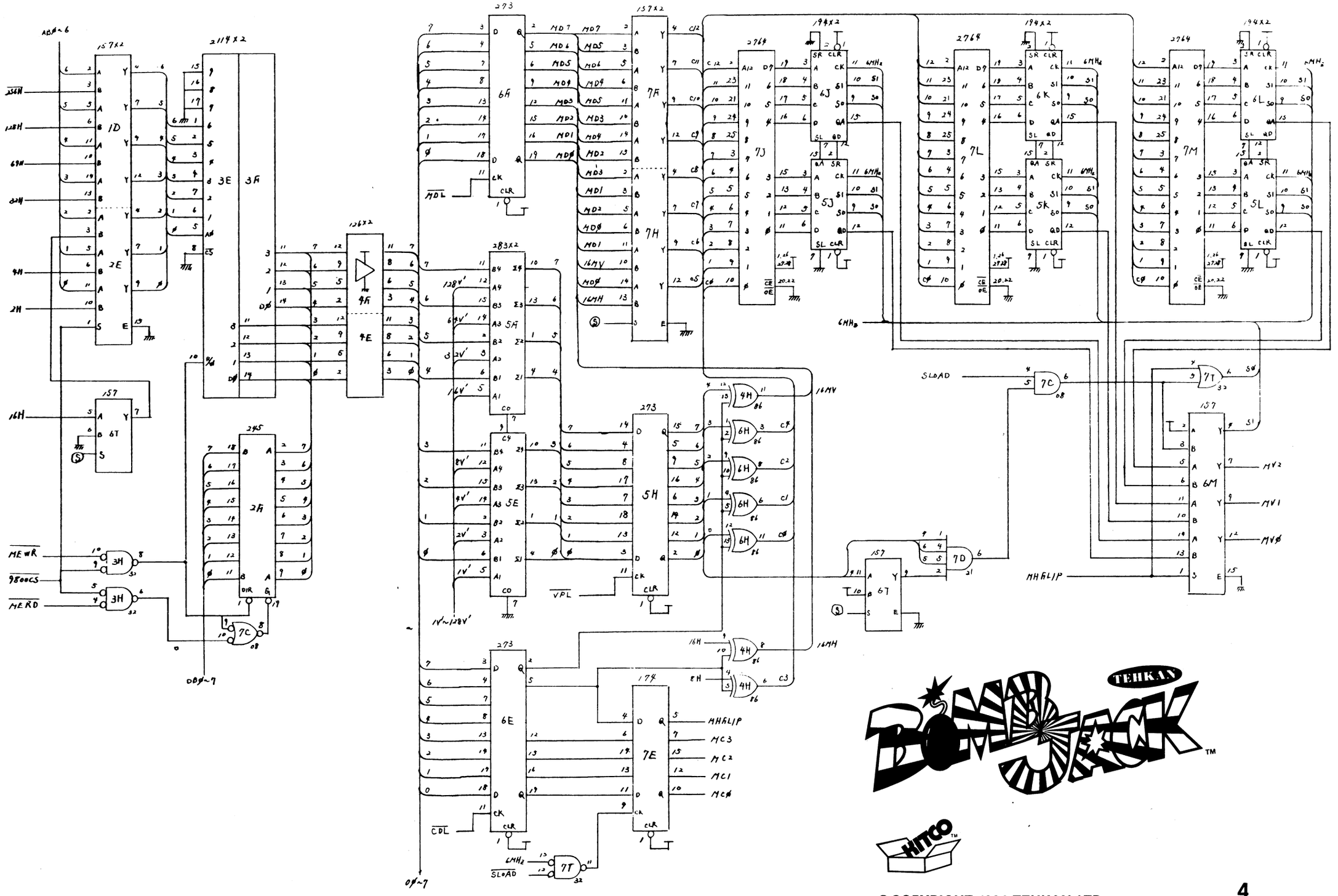

Z80
3K
RESET
WAIT
NMI
INT
BUSRQ
RD
WR
MREQ
IORQ
M1
RASH
MERD
MEWR
126x4
2M
2L
2J
2K
2128 x 2
2764 x 5
1E
1H
1L
1M
1N
1R
2H
6N
6P
7P
7T
3H
SP
5N
VBLANK
WD CLR
NMION
SW
H8L
ROM3
ROM2
ROM1
ROM0
WRAM1
WRAM0
RAM1
RAM0
DB0~DB7


RA1
1KX8
R41
2N
2P
RA2
1KX8
R198
RA3
1KX8
R37
2M
258
RA5
1KX8
SW1
8PDIPSW
2S
2R
RA4
1KX8
SW2
8PDIPSW
258X2
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
AB0
B000,1RD
B0023RD
B0045RD
DB0~7
139
3P
3N
3S
3R
HERD
B000CS
HEWR
B000,5RD
B0023RD
B000,1RD
B000,5WR
B0023WR
B000,1WR
FLIP
NMION
WD CLR
HEWR
B8IOCS
B800H
for
17.18
+5V
R19
470Ω
LED2
15
+12V
R20
1K
LED1
12.13


X2
12.096MHz
R1
R2
C5
3T
3S
3R
3P
3N
4P
4N
5P
5T
6R
6S
6T
7R
7S
7T
7N
2R
2P
2N
1T
2T
1S
1V
2V
4V
8V
16V
32V
64V
128V
VSYNC
1H
2H
4H
8H
16H
32H
64H
128H
256H
HSYNC
VBLANK
CMPBLK
SLOAD
SLT
SL2
SW
SS
HBL
VPL
CPL
MPL
CONTRLDB
CONTRLDA
FLIP
DB0~3



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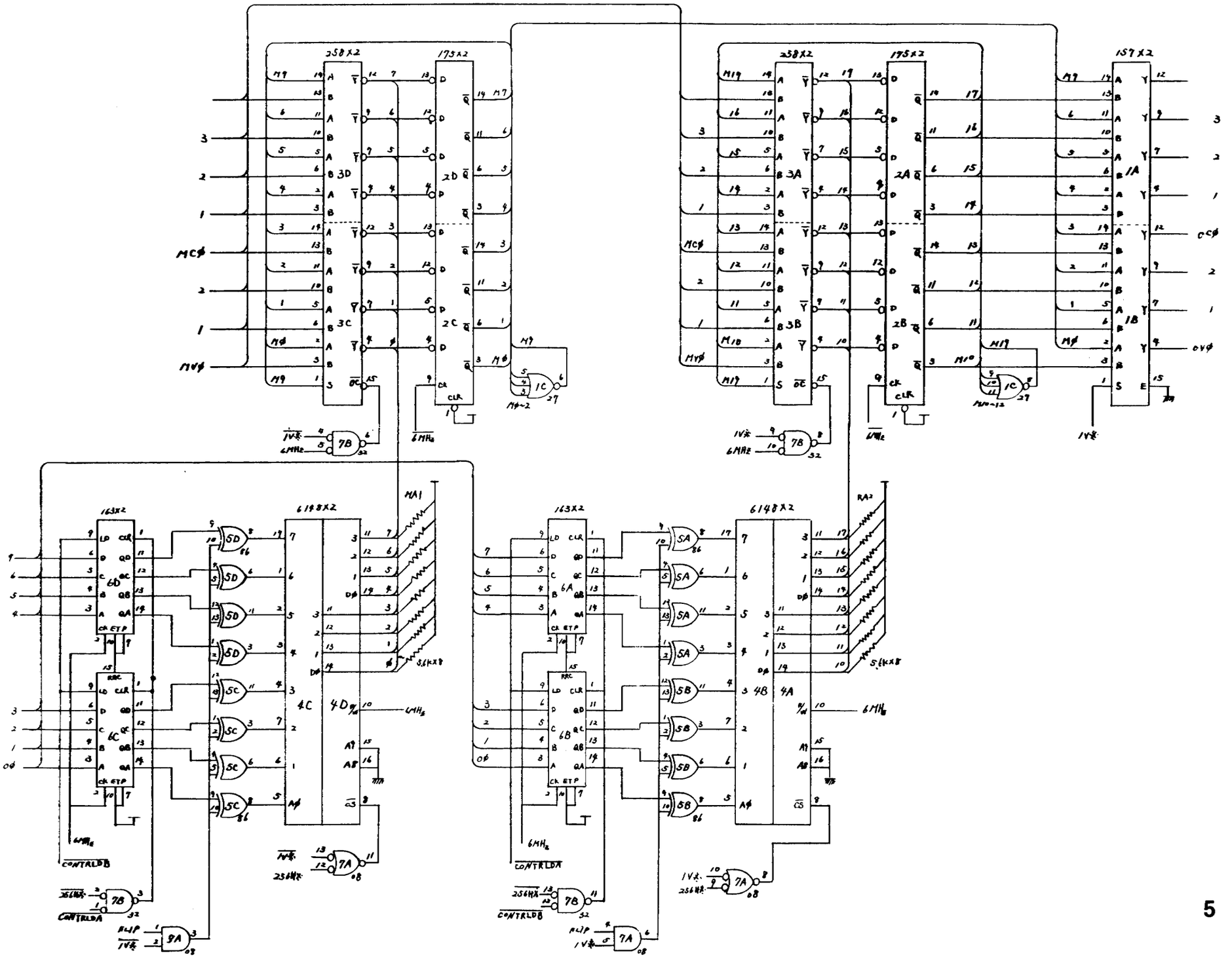
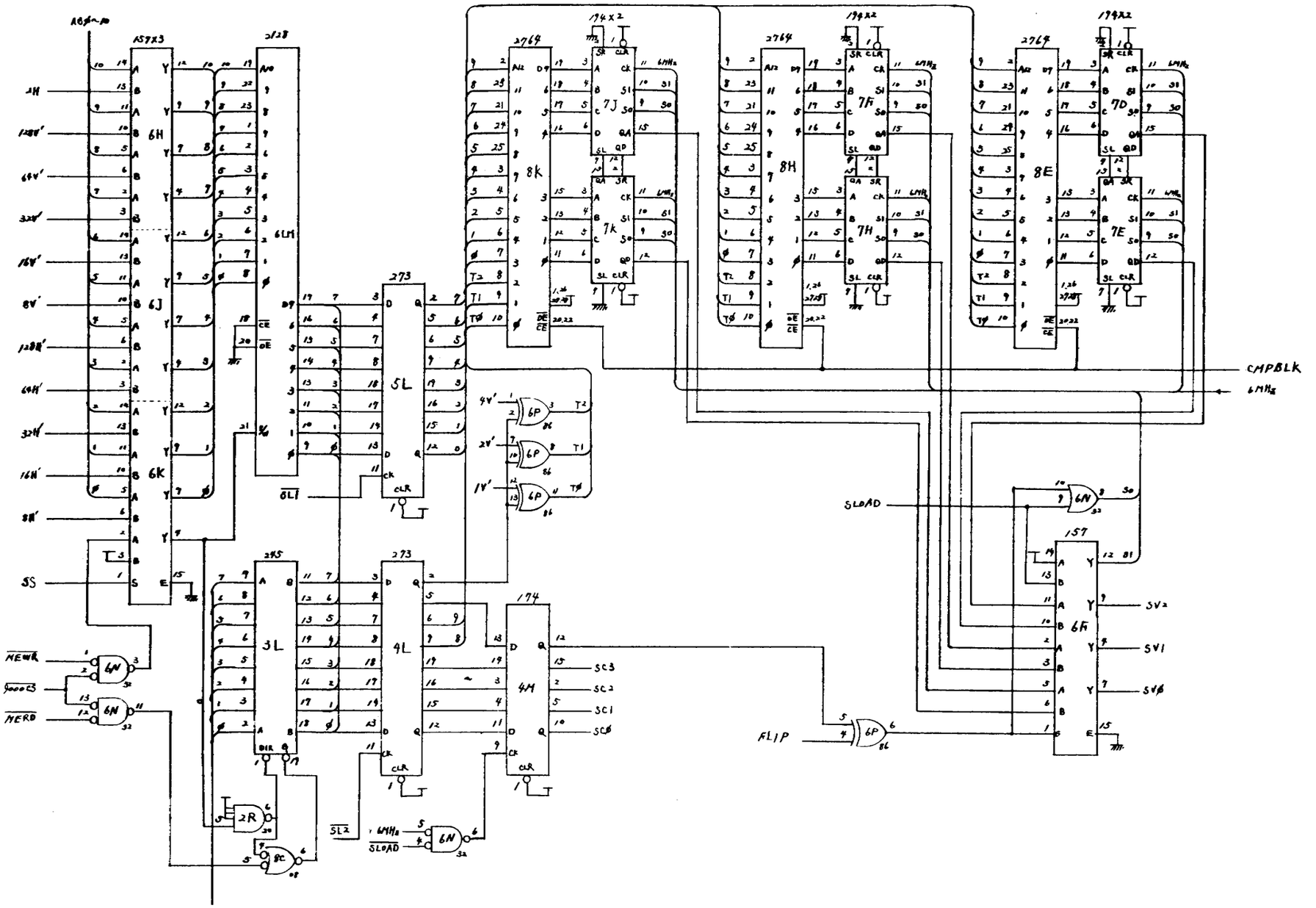
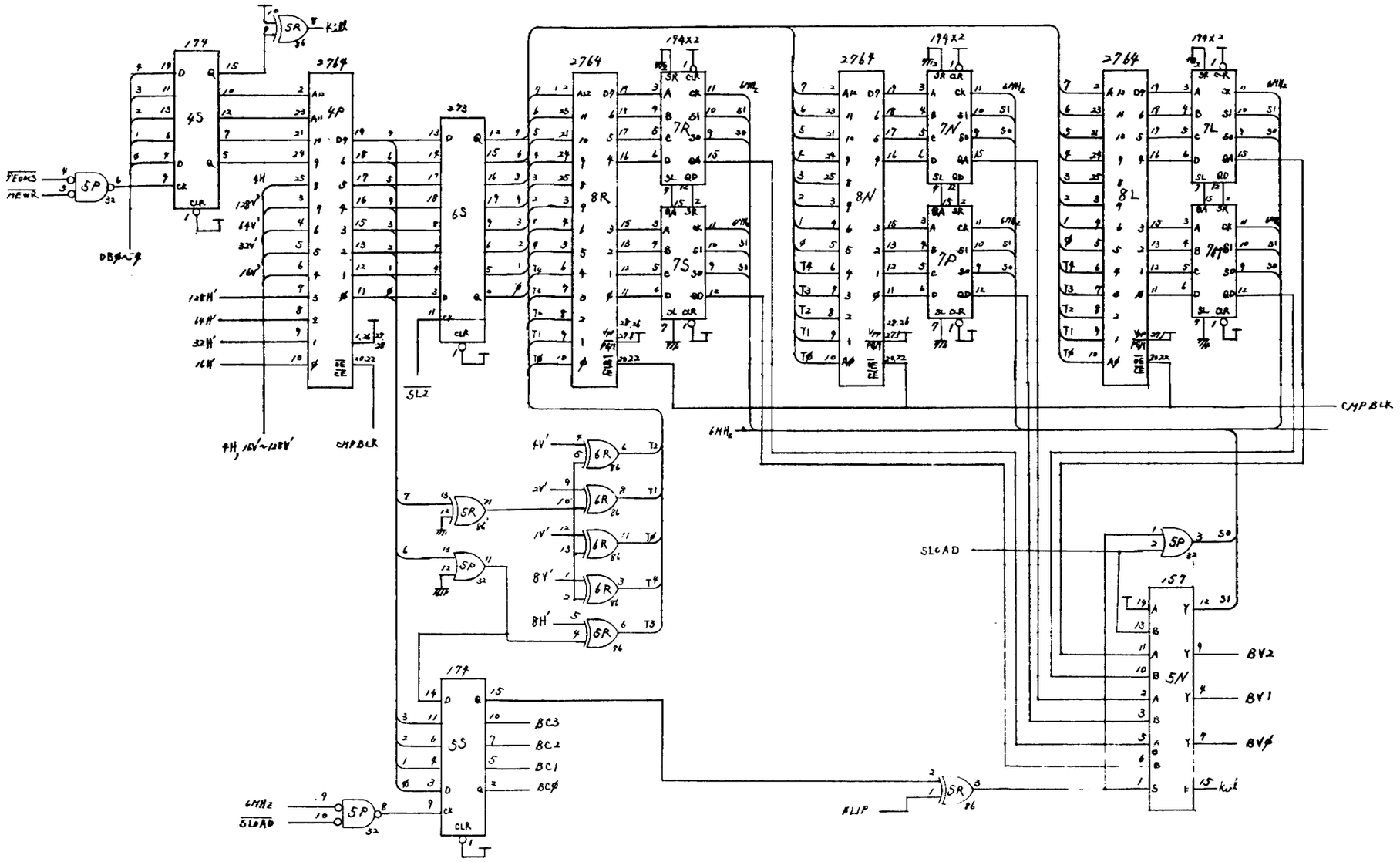
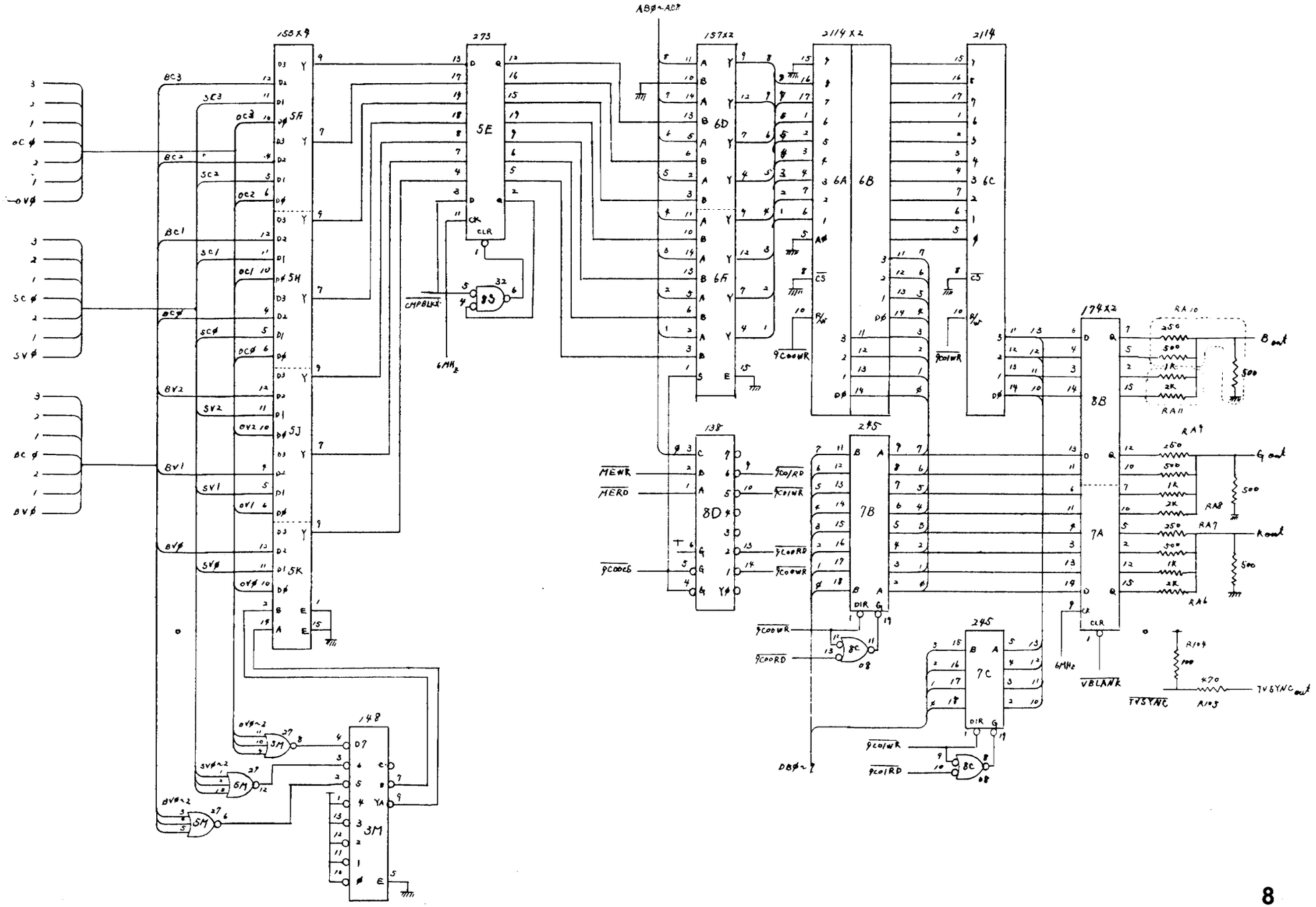
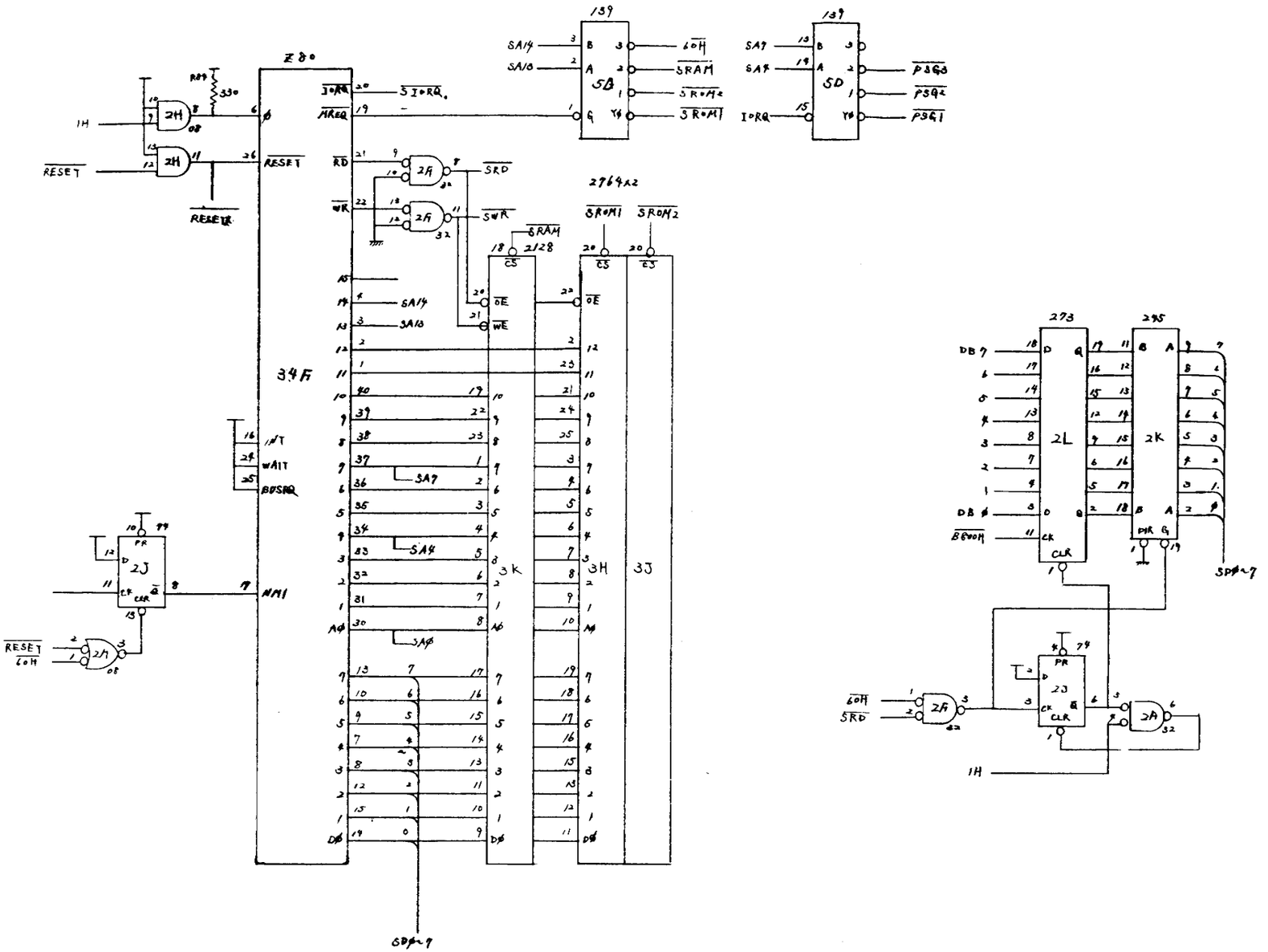
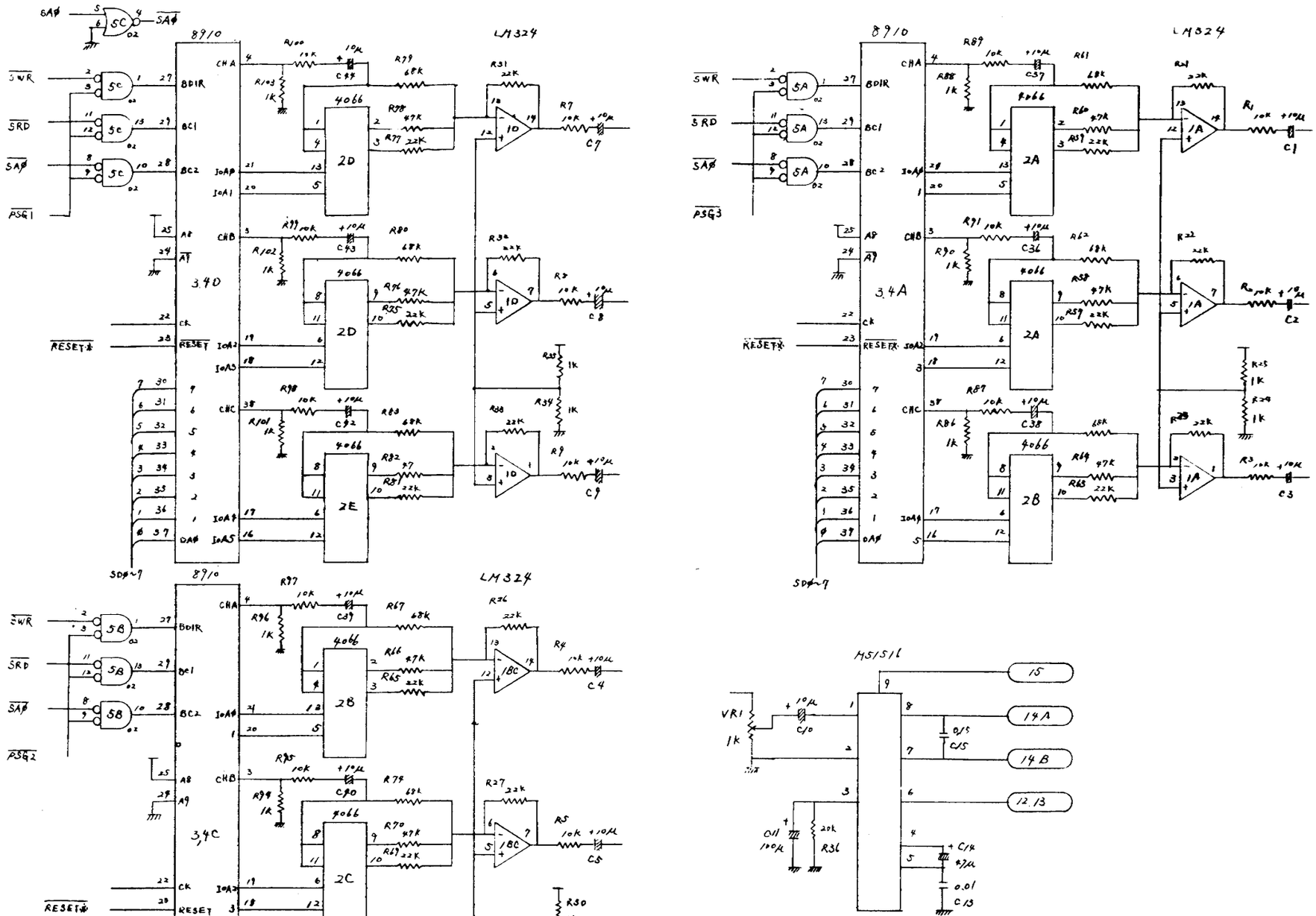

258X2
175X2
157X2
163X2
6148X2
3D
2D
3C
2C
3A
2A
1A
3B
2B
1B
6D
6C
6A
6B
4C
4D
4A
4B
5.6kx8
MA1
RA2
CONTRLDB
CONTRLDA
6MHz
256HR
1V
MCϕ
MVϕ
HCϕ
HVϕ


CMPBLK
6MH2
SLOAD
FLIP
SC3
SC2
SC1
SC0
SV2
SV1
SV0
MEMR
SOUCS
MEMB
SS
SL2
SLI
6MH2
SLOAD


174
4S
2764
4P
273
6S
8R
7R
7S
8N
7N
7P
8L
7L
74X2
SP
SR
6R
157
5N
5S
174
SL2
CMPBLK
SLOAD
FLIP
BC3
BC2
BC1
BCØ
BV2
BV1
BVØ


158X9
273
157X2
2114X2
2114
174X2
138
245
148
5E
6D
6A
6B
6C
6F
8D
8B
7B
7A
7C
5H
5J
5K
5M
3M
32
08
RA10
RA11
RA9
RA8
RA7
RA6
B out
G out
R out
500
250
1K
2K
R104
100
470
R103
TVSYNC out
TVSYNC
VBLANK
6MHz
CMPBLK
MEWR
MERD
PCODES
PCOWR
PCORD
PCOLWR
PCOLRD
DB0~7
AB0~AB?


Z80
34F
3K
3H
3J
2764x2
2128
SRAM
SROM1
SROM2
SRD
SWR
SIORQ
SA14
SA13
SA7
SA6
SA0
SD0~7
1H
RESET
WAIT
BUSRQ
NMI
139
273
245
2L
2K
2J
SP0~7


8910
LM324
3.4D
3.4A
3.4C
2D
2A
2E
2B
2C
4066
SWR
SRD
SAØ
RSG1
RSG3
RSG2
RESETØ
SDØ~7
MS/S/L
VR1
1k
15
14A
14B
12.13