Drawing Package Supplement

to

ASTEROIDS

Operation, Maintenance, and Service Manual

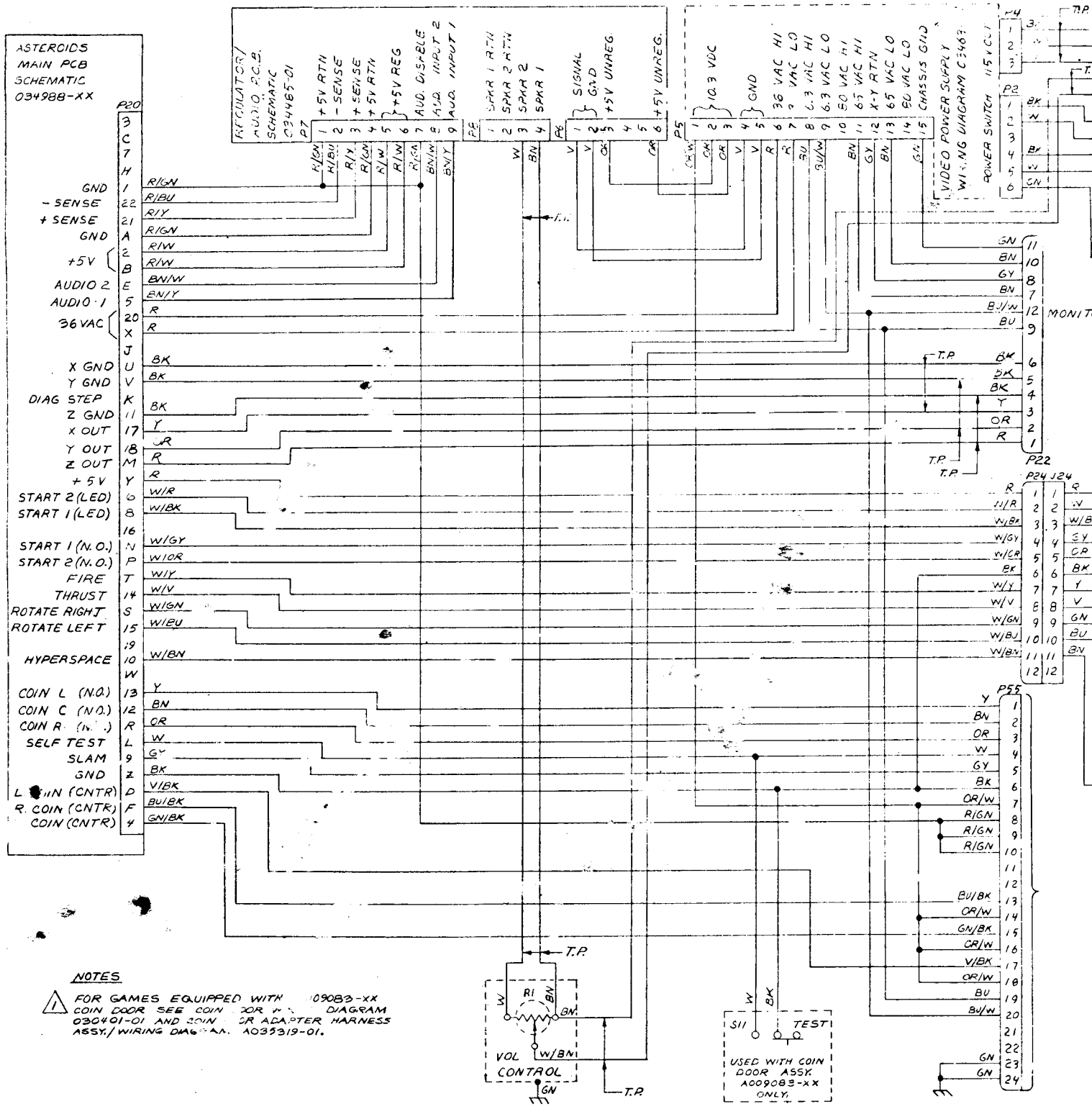
Contents of this Drawing Package

ATARI®

A Warner Communications Company

Sheet 1, Side A
43-01 7th printing

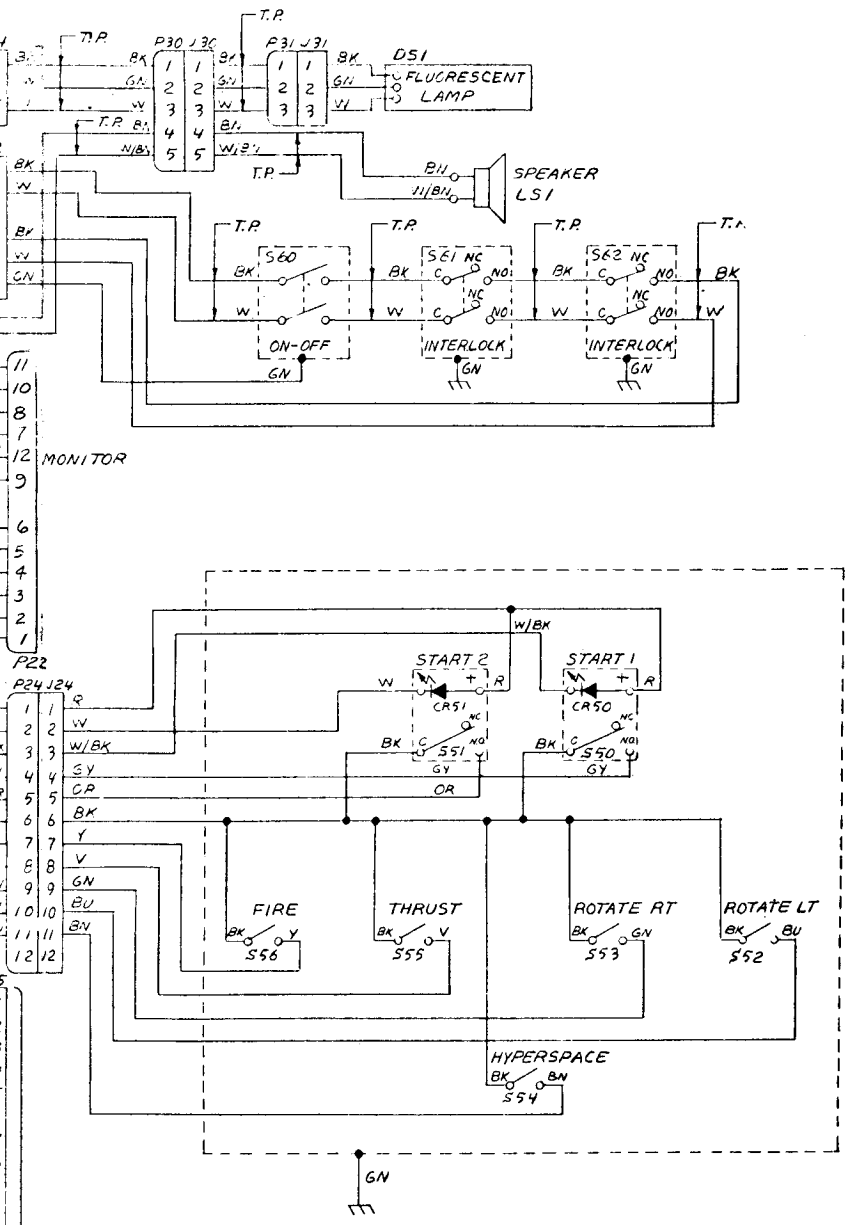
ASTEROIDS WIRING DIAGRAM (035156-02 A)

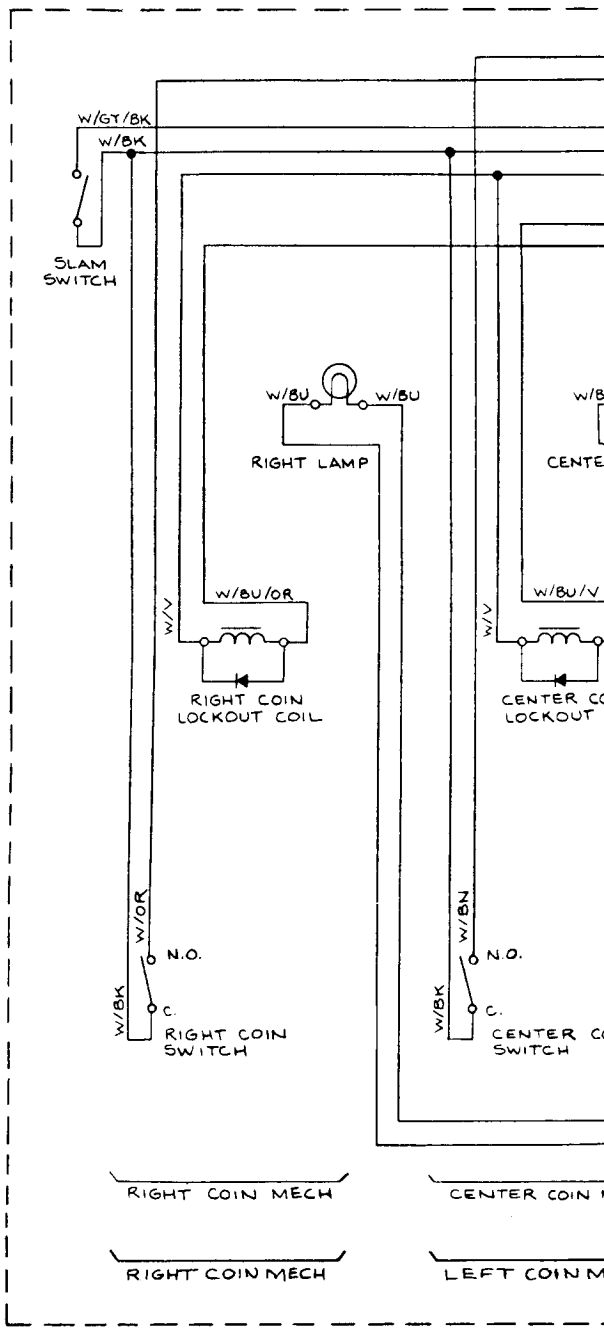


NOTES

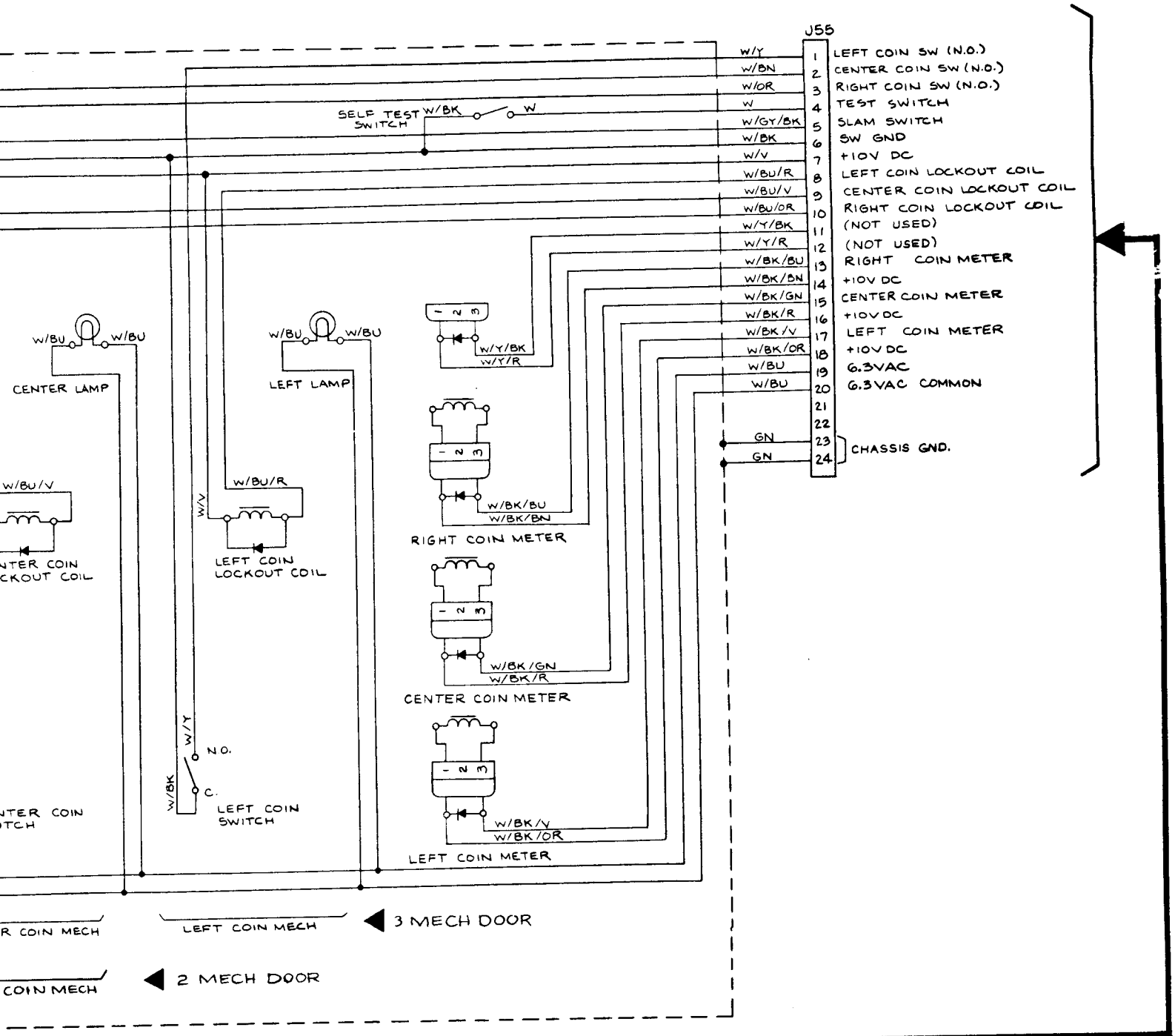
⚠ FOR GAMES EQUIPPED WITH 009083-XX COIN DOOR SEE COIN DOOR WIRING DIAGRAM 030401-01 AND COIN DOOR ADAPTER HARNESS ASSY./WIRING DIAGRAM A035319-01.

COIN DOOR SCHEMATIC (034988-01 A)

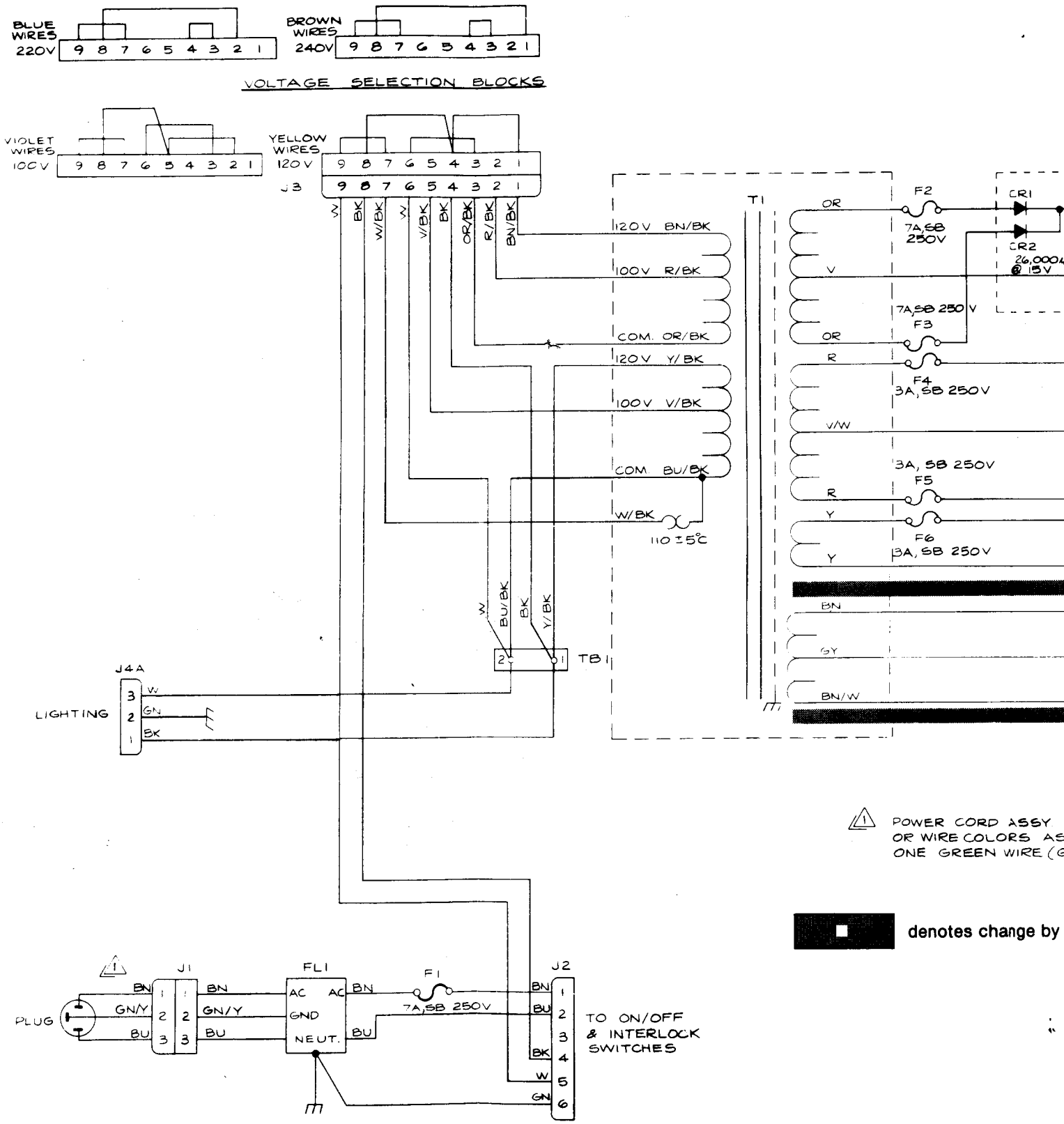


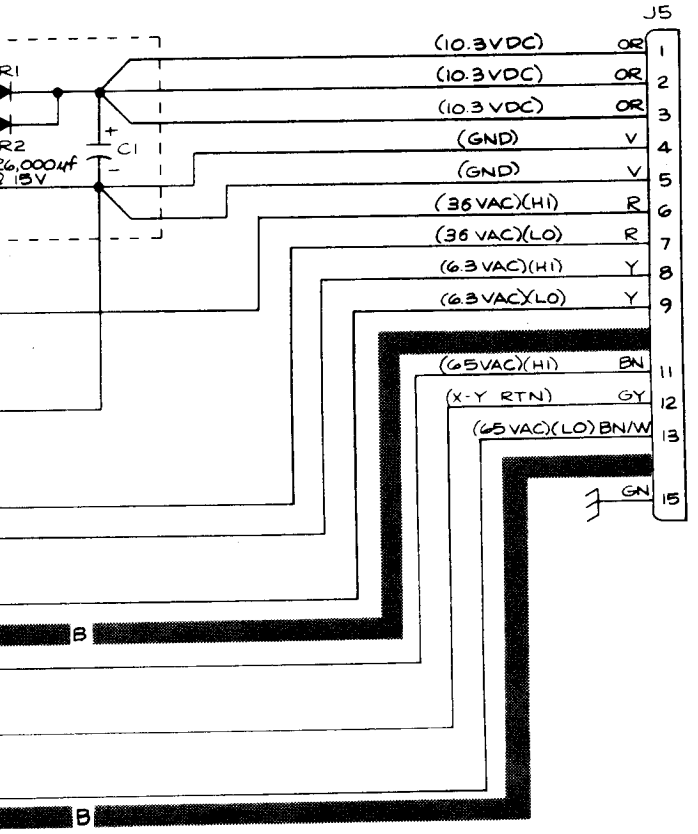


IC


J55
W/Y 1 LEFT COIN SW (N.O.)
W/BN 2 CENTER COIN SW (N.O.)
W/OR 3 RIGHT COIN SW (N.O.)
W 4 TEST SWITCH
W/GY/BK 5 SLAM SWITCH
W/BK 6 SW GND
W/V 7 +10V DC
W/BU/R 8 LEFT COIN LOCKOUT COIL
W/BU/V 9 CENTER COIN LOCKOUT COIL
W/BU/OR 10 RIGHT COIN LOCKOUT COIL
W/Y/BK 11 (NOT USED)
W/Y/R 12 (NOT USED)
W/BK/BU 13 RIGHT COIN METER
W/BK/BN 14 +10V DC
W/BK/GN 15 CENTER COIN METER
W/BK/R 16 +10V DC
W/BK/V 17 LEFT COIN METER
W/BK/OR 18 +10V DC
W/BU 19 6.3VAC
W/BU 20 6.3VAC COMMON
21
22
GN 23
GN 24
CHASSIS GND.
SELF TEST SWITCH
W/BK
W
W/BU
W/BU
CENTER LAMP
W/BU
W/BU
LEFT LAMP
W/Y/BK
W/Y/R
W/BU/V
W/BU/R
W/V
LEFT COIN LOCKOUT COIL
W/BK/BU
W/BK/BN
RIGHT COIN METER
W/BK/GN
W/BK/R
CENTER COIN METER
W/Y
N.O.
W/BK
C.
LEFT COIN SWITCH
W/BK/V
W/BK/OR
LEFT COIN METER
LEFT COIN MECH
3 MECH DOOR
2 MECH DOOR

VIDEO POWER SUPPLY WIRING DIAGRAM (034633-01 B)





SSY MAY HAVE WIRE COLORS AS SHOWN
S AS FOLLOWS: ONE BLACK WIRE (AC),
IRE (GND), AND ONE WHITE WIRE (NEUTRAL).

ge by indicated revision

REGULATOR/AUDIO PCB SCHEMA

Regulator/Audio PCB 034485-01 G

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and −SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

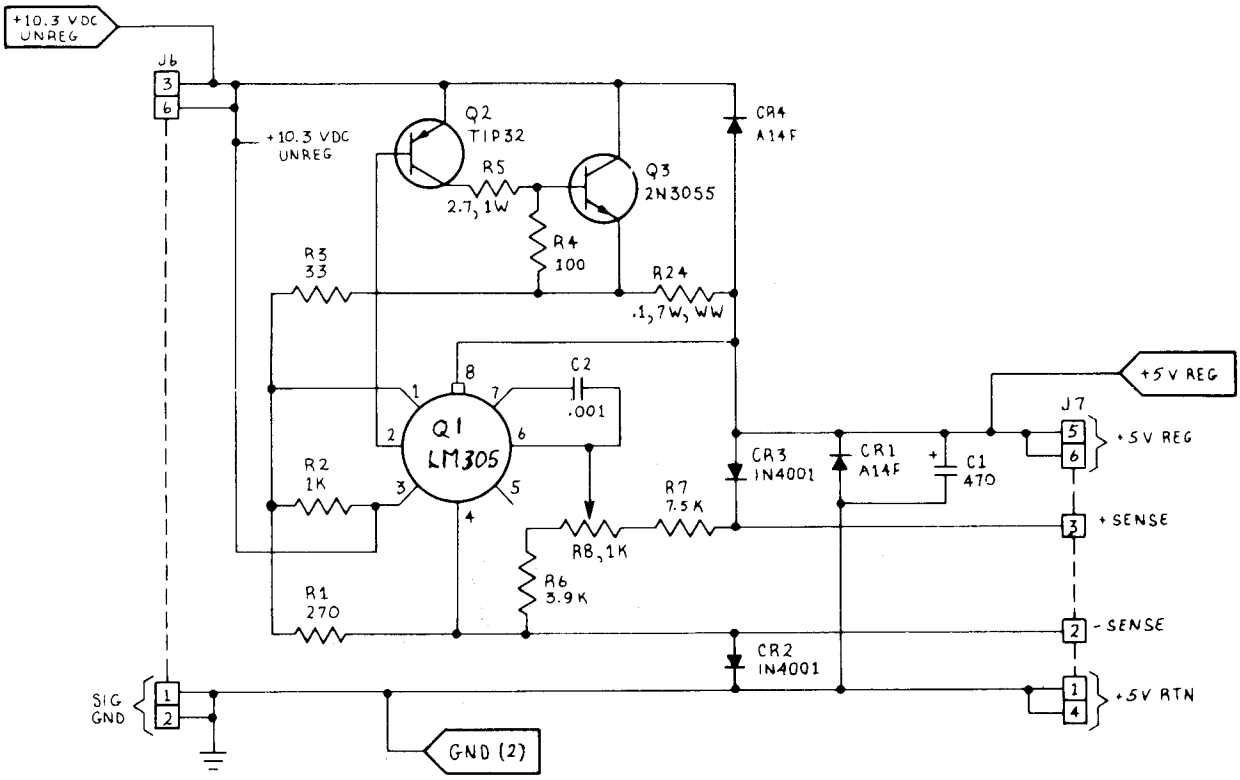
1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

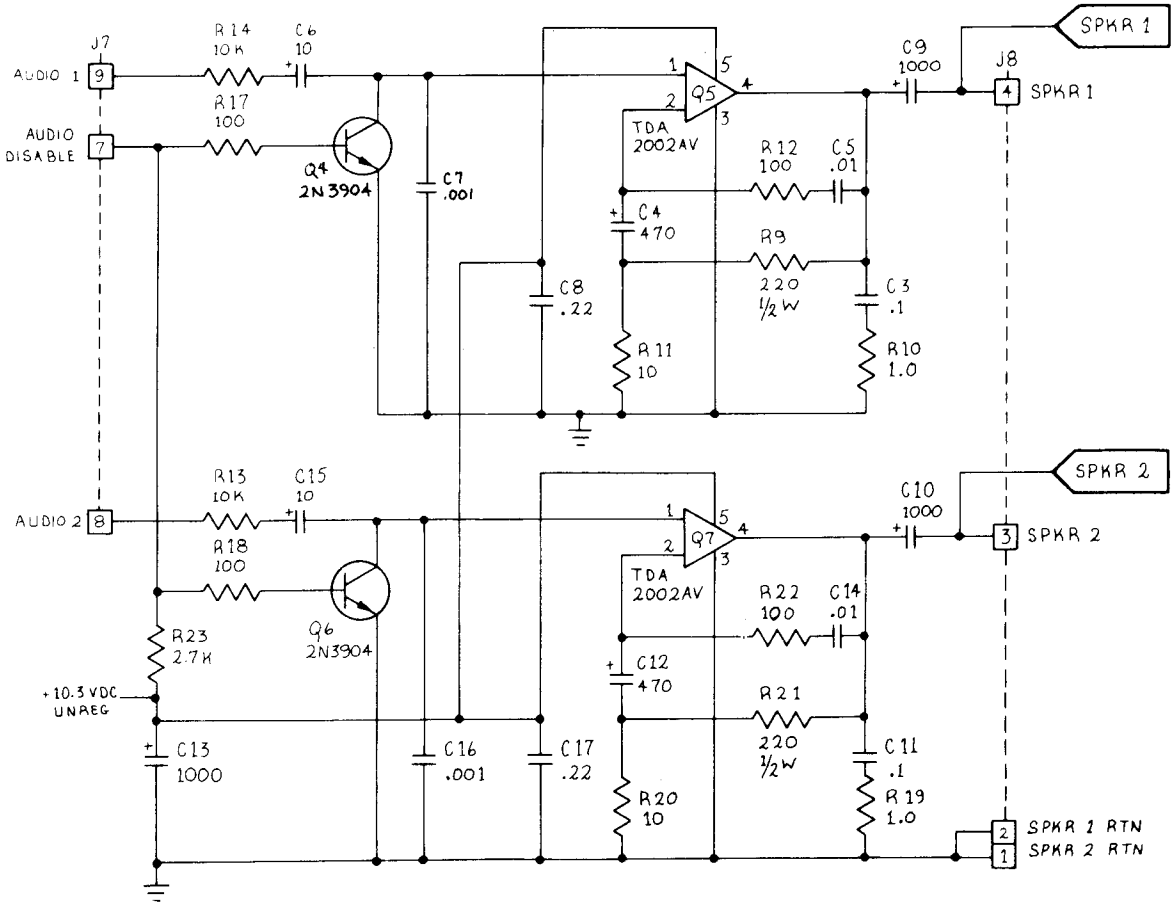
Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten. In Asteroids, the AUDIO DISABLE input to the PCB is permanently grounded. Therefore, this audio circuit is always on, even while the game is in the attract mode.

The audio circuit is repeated on Sheet 2, Side B, including more information about its operation.

TIC (034485-01 G)





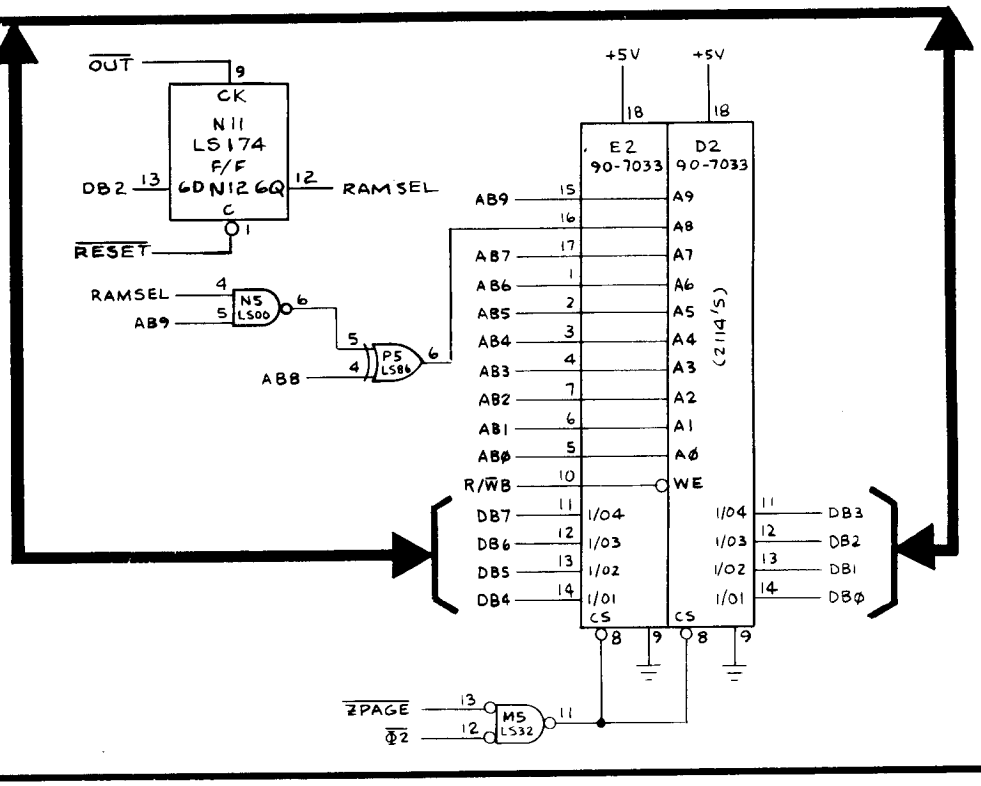
denotes a test point

		0	1	1	1	1	0							1	0	1	W	D									LIFE SOUND NOISE RESET
		0	1	1	1	1	1										W										
		1	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	VECTOR RAM
		1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	VECTOR ROM
		1	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	PROGRAM
		1	1	1	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	

RCUITRY

e RAM is the temporary storage space for MPU and is enabled when $\overline{ZPAGE}$ (Zero enable) is low. When R/$\overline{W}$B (from the is low, the RAM stores the data byte in-DB0 thru DB7) at the location addressed e MPU address bus (AB0 thru AB7). When is high, the MPU reads the stored data at the addressed location.

e signal RAMSEL, when low, has the ef-of swapping pages 2 and 3 within the This allows greater programming flex-.



	-04 P.C. Boards (ROMs)		-05 and -06 P.C. Boards (ROMs)	
	035143-02	C1	035143-02	E/F2
	035144-02	D/E1	035144-02	H2
	035145-02	F1	035145-02	J2

ATARI®

A Warner Communications Company

Sheet 1, Side B

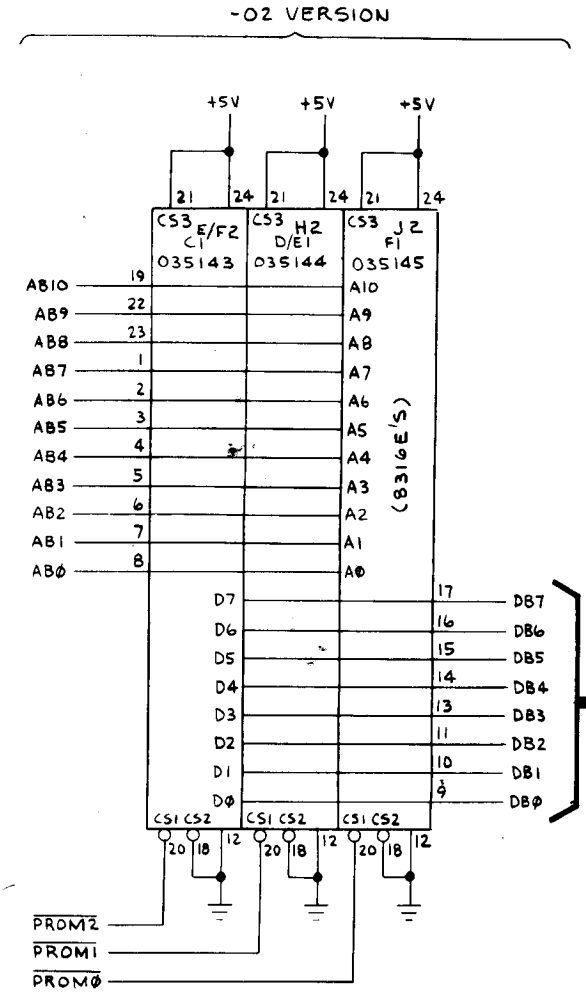
ASTEROIDS Microprocessor

Section of 034986-01 thru -04 H
034986-05 and -06 B

NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT ENCLOSED IN PARENTHESIS ARE FOR 74LS245. PIN NUMBERS IN PARENTHESIS ARE FOR AN AM8304B.

3E00
4000-47FF
5000-57FF
6800-7FFF

Asteroids game is con-
version of the PCB or
the PCB. One ROM is
ll PROMs connected to
removed before replac-
ble, remove PROMs at
before replacing with



NOTE:

All reference designations in red are for the -05 and -06 PCB assemblies only. For example, the 8316E ROM above is at location F1 on the -01 thru -04 PCB, but is at location J2 on a -05 and -06 PCB.

The reference designations, used in the circuit descriptions, refer to the -01 thru -04 PCB assemblies only.

RAM CIR

The R
the MPU
Page en
MPU) is
put (DB0
by the M
R/WB is
byte at t

The si
fect of
RAM. Th
ibility.

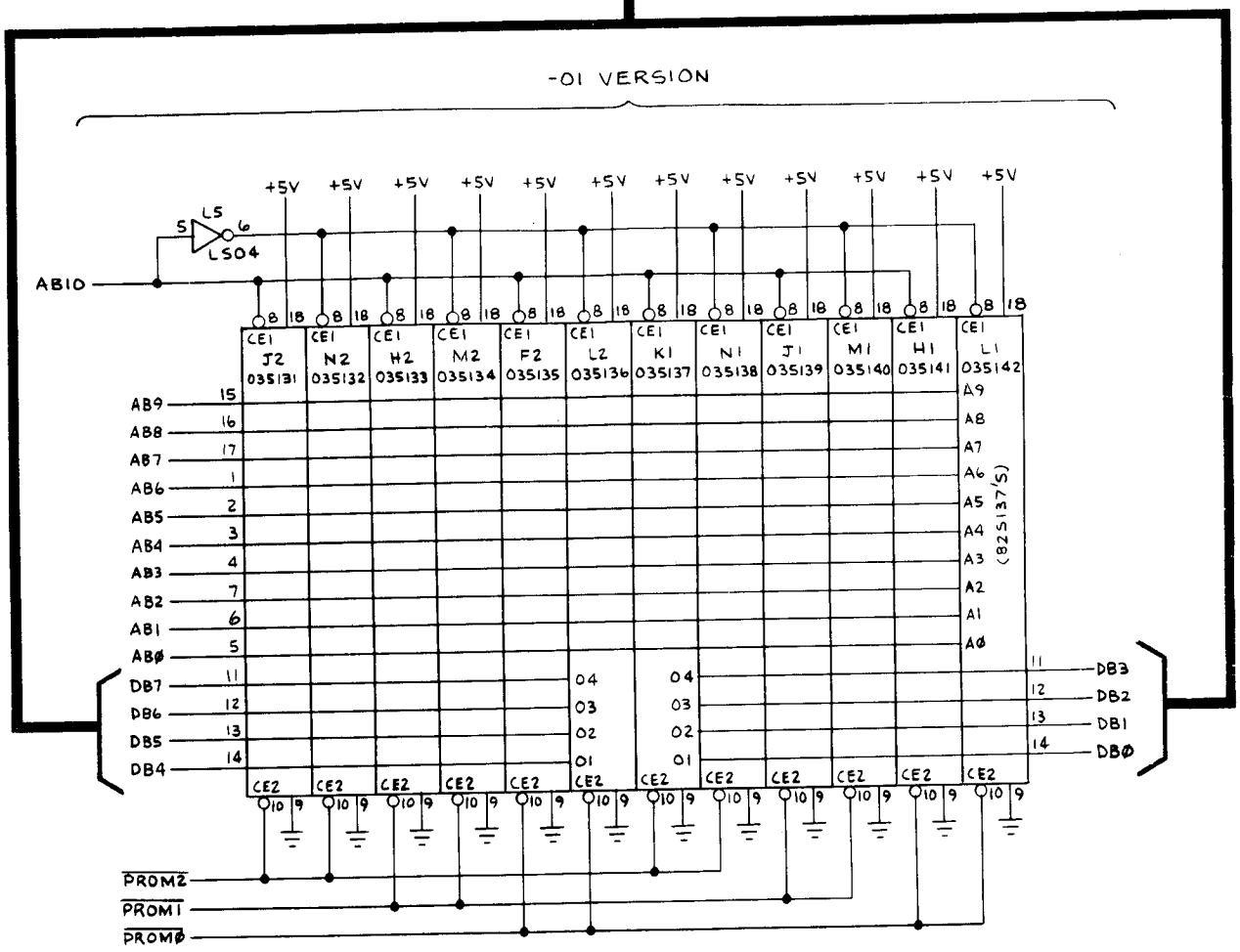
-03 P.C. Boards (PROMs)	Alternate -03 P.C. Boards (PROMs)
035131-02 J2 035132-02 N2	035150-02 J2
035137-02 K1 035138-02 N1	035153-02 K1
035133-02 H2 035134-02 M2	035151-02 H2
035139-02 J1 035140-02 M1	035154-02 J1
035135-02 F2 035136-02 L2	035152-02 F2
035141-02 H1 035142-02 L1	035155-02 L1

The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

FROM SWITCH INPUTS
SHEET 2, SIDE B

ROM/PROM CIRCUITRY

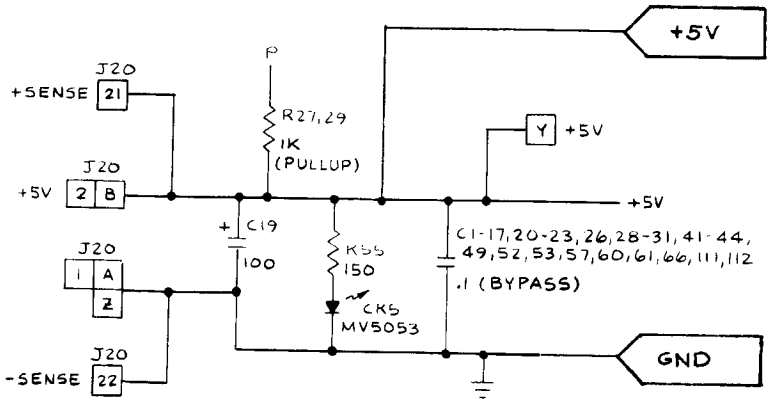
Program Memory for the Asteroid
tained in PROMs for the -01 version
ROMs for the -02 version of the PCI
equivalent to four PROMs. All PROM
a common enable must be removed
ing with a ROM. For example, rem
locations F2, H1, L2 and L1 before
ROM at location F1.



denotes change by indica ec

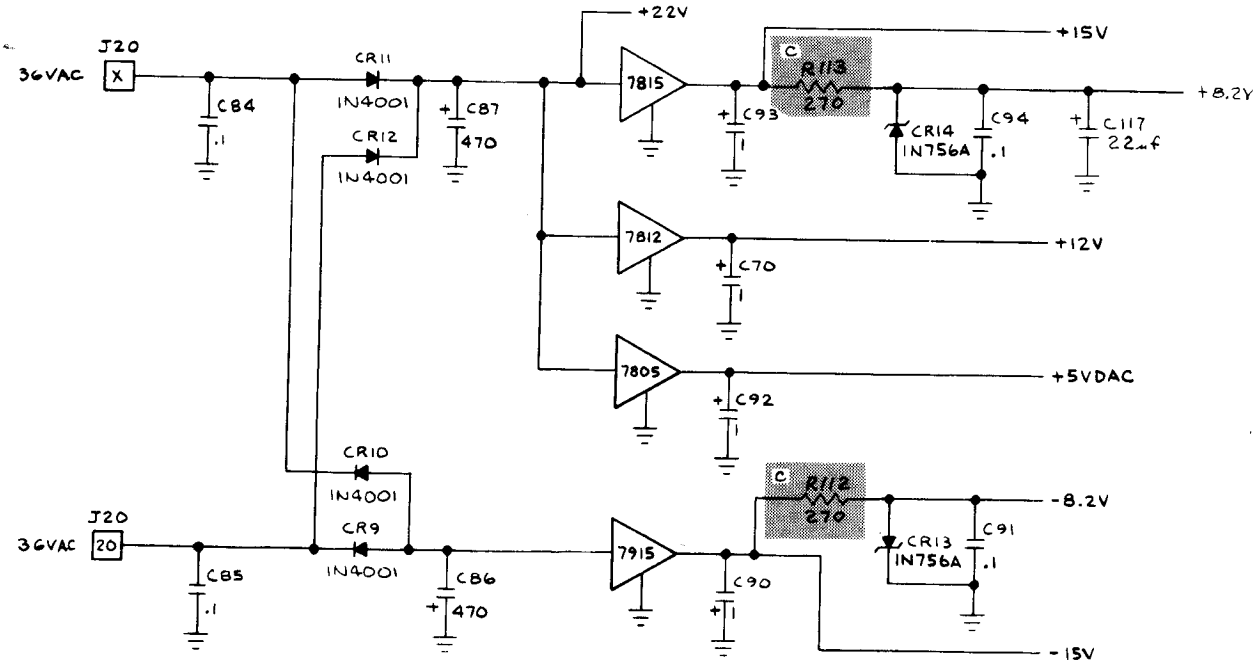
denotes a test point

POWER INPUT

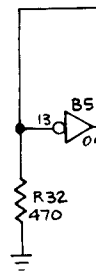


This circuitry consists of the PCB inputs and outputs for the +5 VDC logic power and 36 VAC input to the on board regulators. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 36 VAC inputs are received by two full wave rectifiers. Diodes CR9 and CR10 rectify the negative cycle of the input and the 7915 regulates the voltage at −15 VDC. Diodes CR11 and CR12 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional 5 VDC for the DACs. Zener diode CR14 supplies the +8.2 VDC for the sample and hold circuit. The +22V (unregulated) is used to power operational amplifiers P11 and L8 in the audio output.

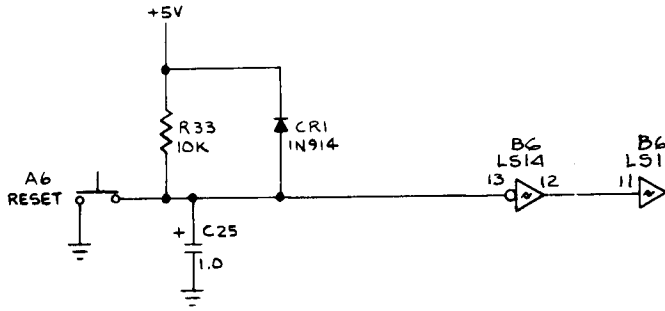


CLOCK CIRCUIT



The clock circuit consists o
verters and counters C4 and B4
crystal frequency down to the
Asteroids game.

POWER RESET AN

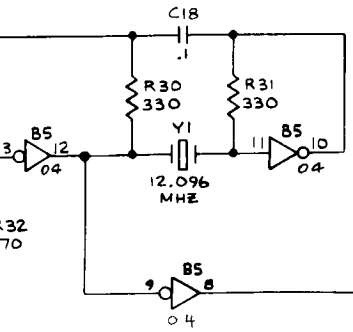


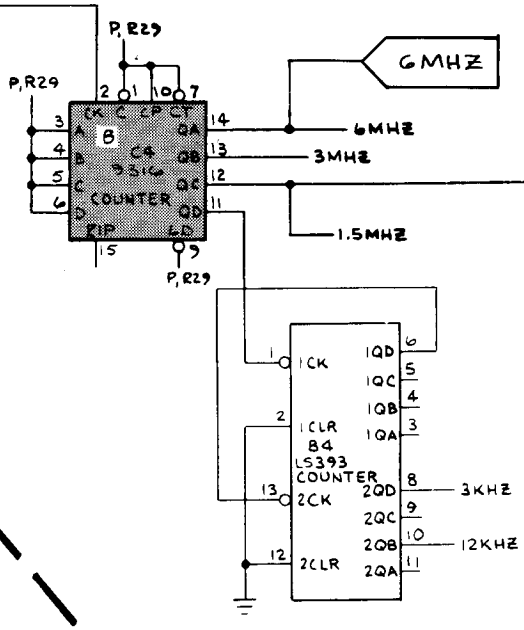
During inital power-up, the delayed charging of capacitor C25 causes a preset of flip-flop D4 and a clear of counter D5. This results in holding $\overline{\text{RESET}}$ input to the MPU low. When the charge of C25 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and $\overline{\text{RESET}}$ is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the $\overline{\text{WDCLR}}$ (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the $\overline{\text{RESET}}$ condition. If the MPU program strays from its intended sequence and does not output the $\overline{\text{WDCLR}}$ signal, counter D5 will count up to the $\overline{\text{RESET}}$ state and cause the MPU to return to its initialization routine.

denotes change by indicated revis

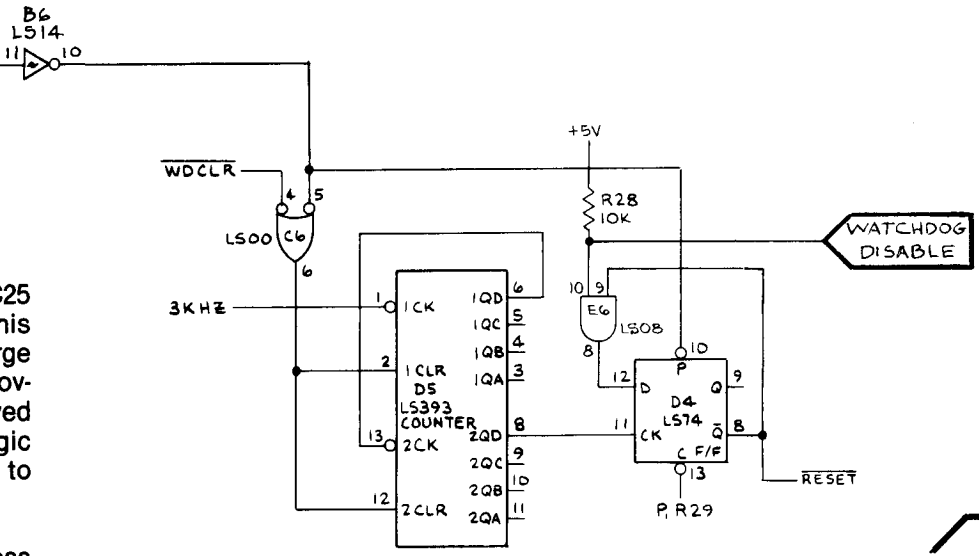
NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY OF 1.5 MHZ. THEREFORE THE MPU CHIP MUST BE 6502A. THE 6502'S MAXIMUM FREQUENCY IS 1 MHZ AND IS NOT COMPATIBLE WITH THIS GAME.



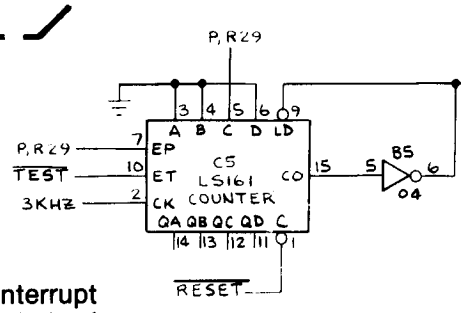


sts of crystal Y1 and associated in-
d B4. Counters C4 and B4 count the
the frequencies necessary for the

AND WATCHDOG COUNTER

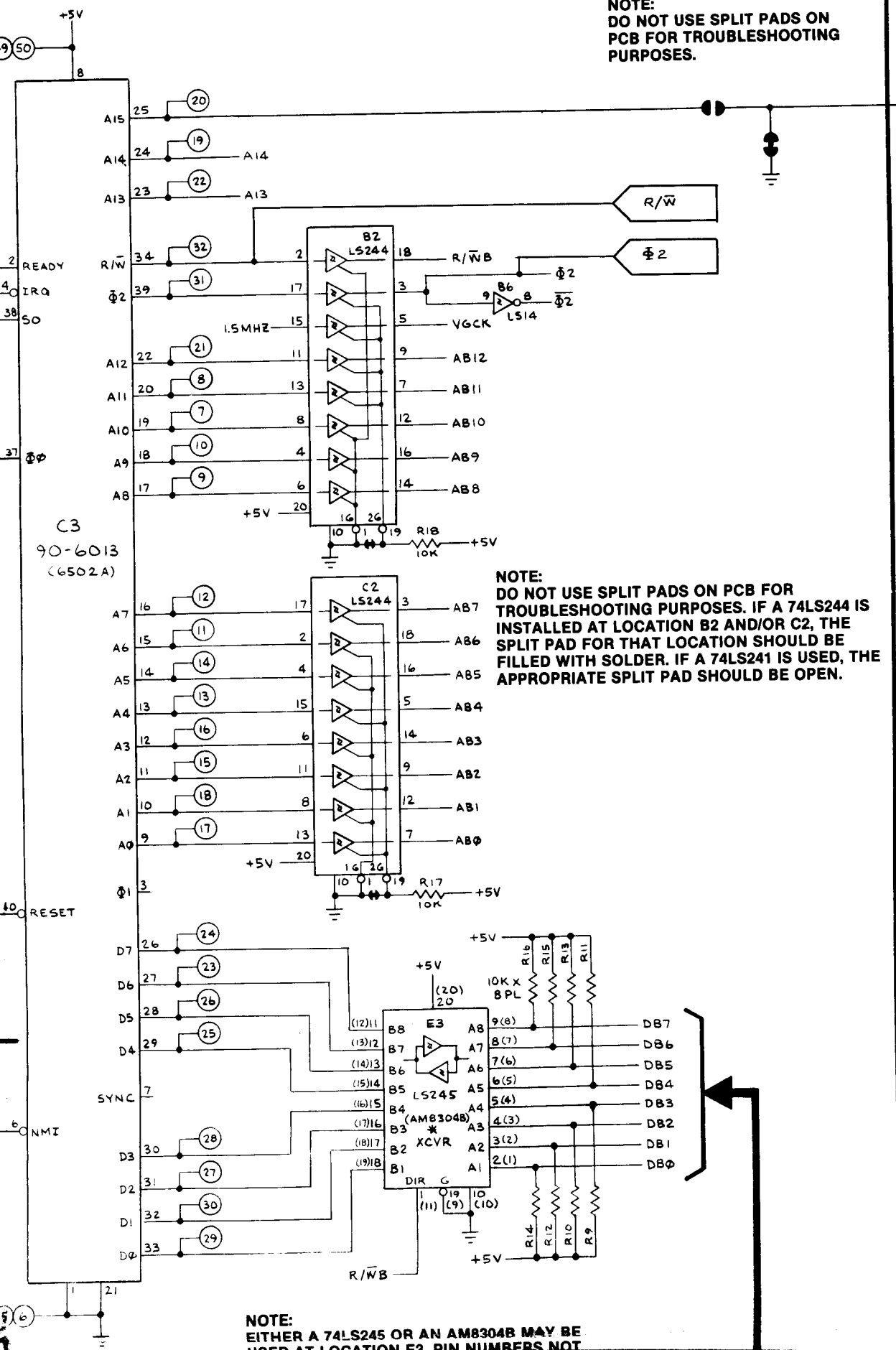


NMI COUNTER



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up,

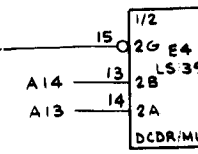
MPU CIRCUITRY



NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES. IF A 74LS244 IS INSTALLED AT LOCATION B2 AND/OR C2, THE SPLIT PAD FOR THAT LOCATION SHOULD BE FILLED WITH SOLDER. IF A 74LS241 IS USED, THE APPROPRIATE SPLIT PAD SHOULD BE OPEN.

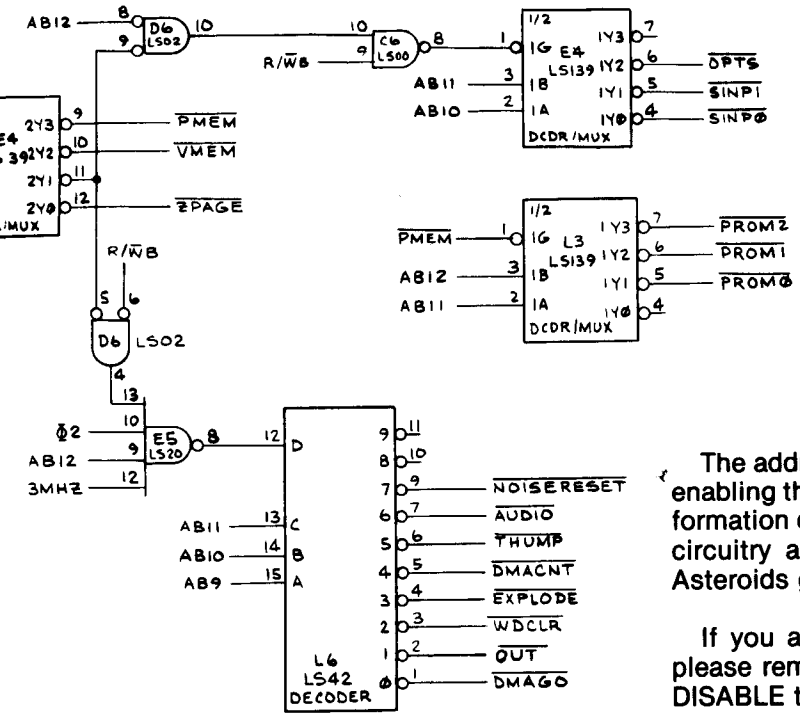
NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT

ADDRESS D



HEXADECIMAL	A15
0000-01FF	
0200-02FF	
0300-03FF	
2001	
2002	
2003	
2004	
2005	
2006	
2007	
2400	
2401	
2402	
2403	
2404	
2405	
2406	
2407	
2800	
2801	
2802	
2803	
3000	
3200	
3200	
3200	
3200	
3200	
3200	
3400	
3600	
3600	
3A00	
3A00	
3C00	
3C01	
3C02	
3C03	
3C04	
3C05	
3E00	
4000-47FF	
5000-57FF	
6800-7FFF	

DECODING CIRCUITRY



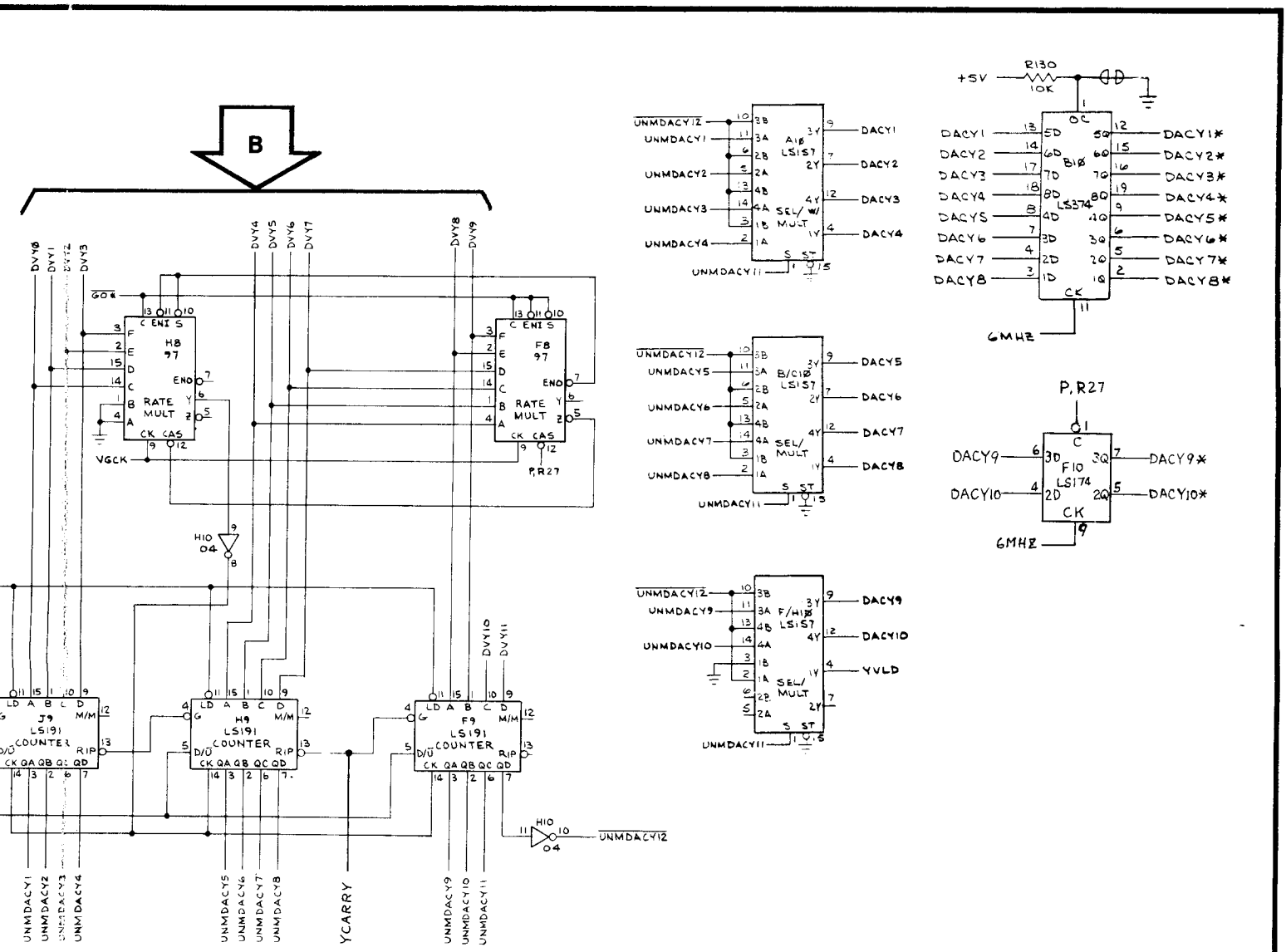
The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids game.

If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

ADDRESS																	DATA								
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0				0	1	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	ZERO & ONE PAGE RAM
	0	0				1	0	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	PLAYER 1 RAM
	0	0				1	1	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	PLAYER 2 RAM
	0	1	0	0	0								0	0	1	R	D								3 KHz
	0	1	0	0	0								0	1	0	R	D								HALT
	0	1	0	0	0								0	1	1	R	D								HYPERSPACE SW
	0	1	0	0	0								1	0	0	R	D								FIRE SW
	0	1	0	0	0								1	0	1	R	D								DIAG. STEP
	0	1	0	0	0								1	1	0	R	D								SLAM SW
	0	1	0	0	0								1	1	1	R	D								SELF TEST SW
	0	1	0	0	1								0	0	0	R	D								LEFT COIN SW
	0	1	0	0	1								0	0	1	R	D								CENTER COIN SW
	0	1	0	0	1								0	1	0	R	D								RIGHT COIN SW
	0	1	0	0	1								0	1	1	R	D								1 PLYR START SW
	0	1	0	0	1								1	0	0	R	D								2 PLYR START SW
	0	1	0	0	1								1	0	1	R	D								THRUST SW
	0	1	0	0	1								1	1	0	R	D								ROT RIGHT SW
	0	1	0	0	1								1	1	1	R	D								ROT LEFT SW
	0	1	0	1	0									0	0	R							D	D	OPT SW (SW8, SW7)
	0	1	0	1	0									0	1	R							D	D	OPT SW (SW6, SW5)
	0	1	0	1	0									1	0	R							D	D	OPT SW (SW4, SW3)
	0	1	0	1	0									1	1	R							D	D	OPT SW (SW2, SW1)
	0	1	1	0	0	0										W									DMAGO
	0	1	1	0	0	1										W								D	2 PLYR START LAMP
	0	1	1	0	0	1										W							D		1 PLYR START LAMP
	0	1	1	0	0	1										W						D			RAMSEL
	0	1	1	0	0	1										W					D				COIN CNTRL LEFT
	0	1	1	0	0	1										W				D					COIN CNTRC CENTER
	0	1	1	0	0	1										W			D						COIN CNTRR RIGHT
	0	0	1	0	1	0										W									WDCLR
	0	1	1	0	1	1										W	D	D							EXPLOSION PITCH
	0	1	1	0	1	1										W			D	D	D	D			EXPLOSION VOLUME
	0	1	1	1	0	0										W				D					THUMP VOLUME
	0	1	1	1	0	0										W					D	D	D	D	THUMP FREQUENCY
	0	1	1	1	1	0							0	0	0	W	D								SAUCER SOUND
	0	1	1	1	1	0							0	0	1	W	D								SAUCER FIRE SOUND
	0	1	1	1	1	0							0	1	0	W	D								SAUCER SOUND SELECT
	0	1	1	1	1	0							0	1	1	W	D								SHIP THRUST SOUND
	0	1	1	1	1	0							1	0	0	W	D								SHIP FIRE SOUND
	0	1	1	1	1	0							1	0	1	W	D								LIFE SOUND
	0	1	1	1	1	1										W									NOISE RESET
	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	VECTOR RAM
	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	VECTOR ROM

Latch 1 is cleared by ALPHANUM.

ndicated revision



ers count up or down. DVX11 is used multiplexers D10, E10, and F10.
ACX10 (X axis unmultiplexed digital-are transferred to the output of the outputs of the latches on each rising the microcomputer clock circuitry). gnals are sent to the digital-to-analog eo output.
outputs represent the physical place-tor. The far left of the monitor screen e far right is 1023. Therefore, if the was greater than 1023, the monitor ide of the screen and start again on wraparound" condition. To prevent a select input from UNMDACX11 goes than 1023 or less than 0. This selects the multiplexers to the DACs, forc-thus keeping the beam on the ap-nstead of allowing it to wraparound. valid) outputs from the X and Y posi-atched and gated together to enable valid).

Sheet 2, Side A

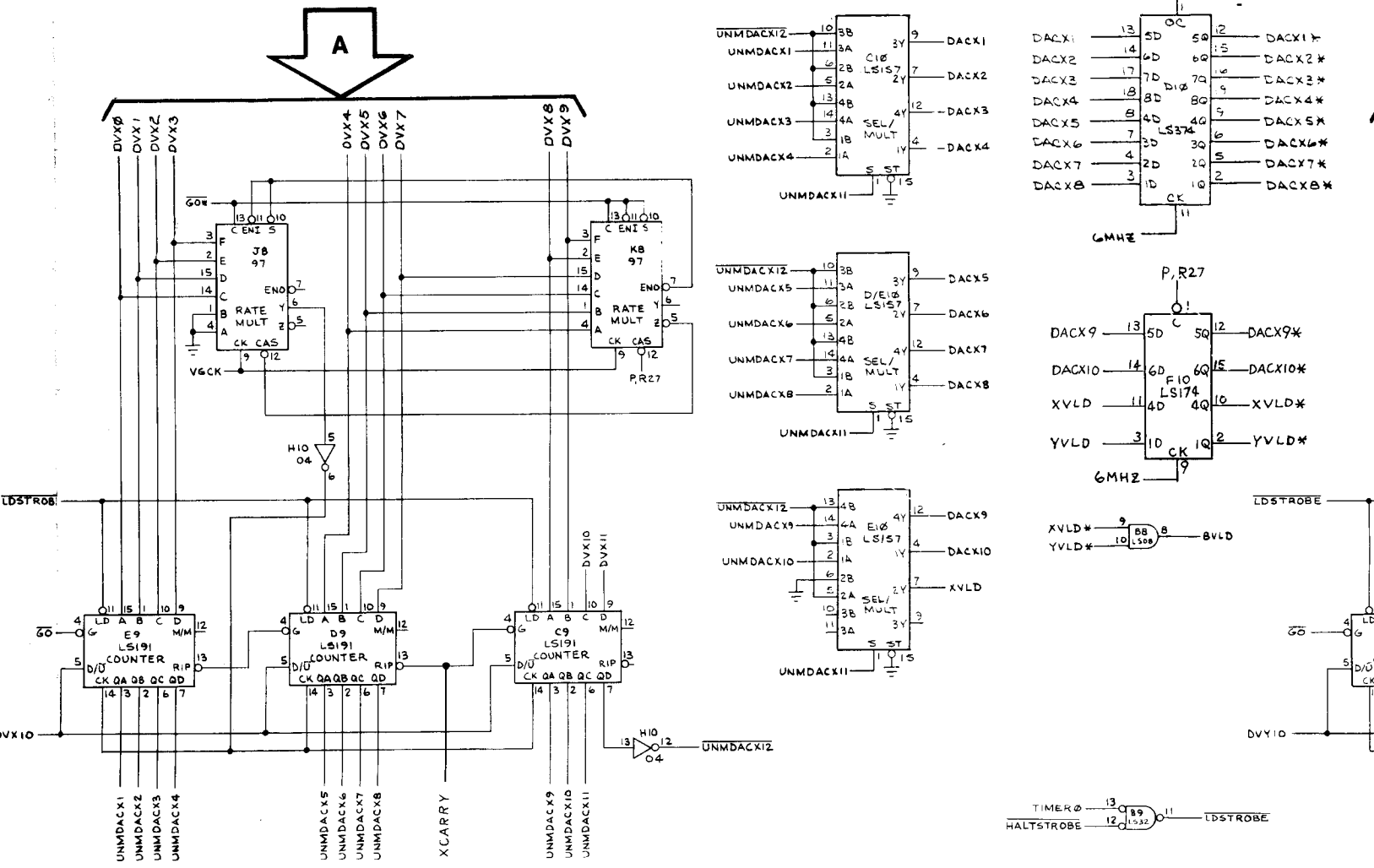
COCKTAIL ASTEROIDS

Video Generator Section of 034986-XX G

ATARI®

A Warner Communications Company

X AND Y POSITION COUNTERS



ounter are two identical circuits. criptiondiscusses only the X position

contain rate multipliers (J8 and K8), d E9), multiplexers (D10, E10, and F10), nd H10. The output of the down/up umberthat represents the horizontal monitoscreen (or X axis), with 0 being and 1023 being the far right side of the asing this binary number output will e rightor left, respectively. The vector codes instructions from its memory, that data to alter the binary count of ways.

eset these counters to an entirely dif- eviouscontents. This will cause the cationon the monitor screen instan- new vector from a different starting ious vector ended. While the beam is "jumping" to this new position, the beam itself is turned off to prevent unwanted lines from appearing on the screen. To preset this new position into the counters, the state generator causes LDSTROBE to go low. At this time, a new 12-bit number (DVX0-11) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

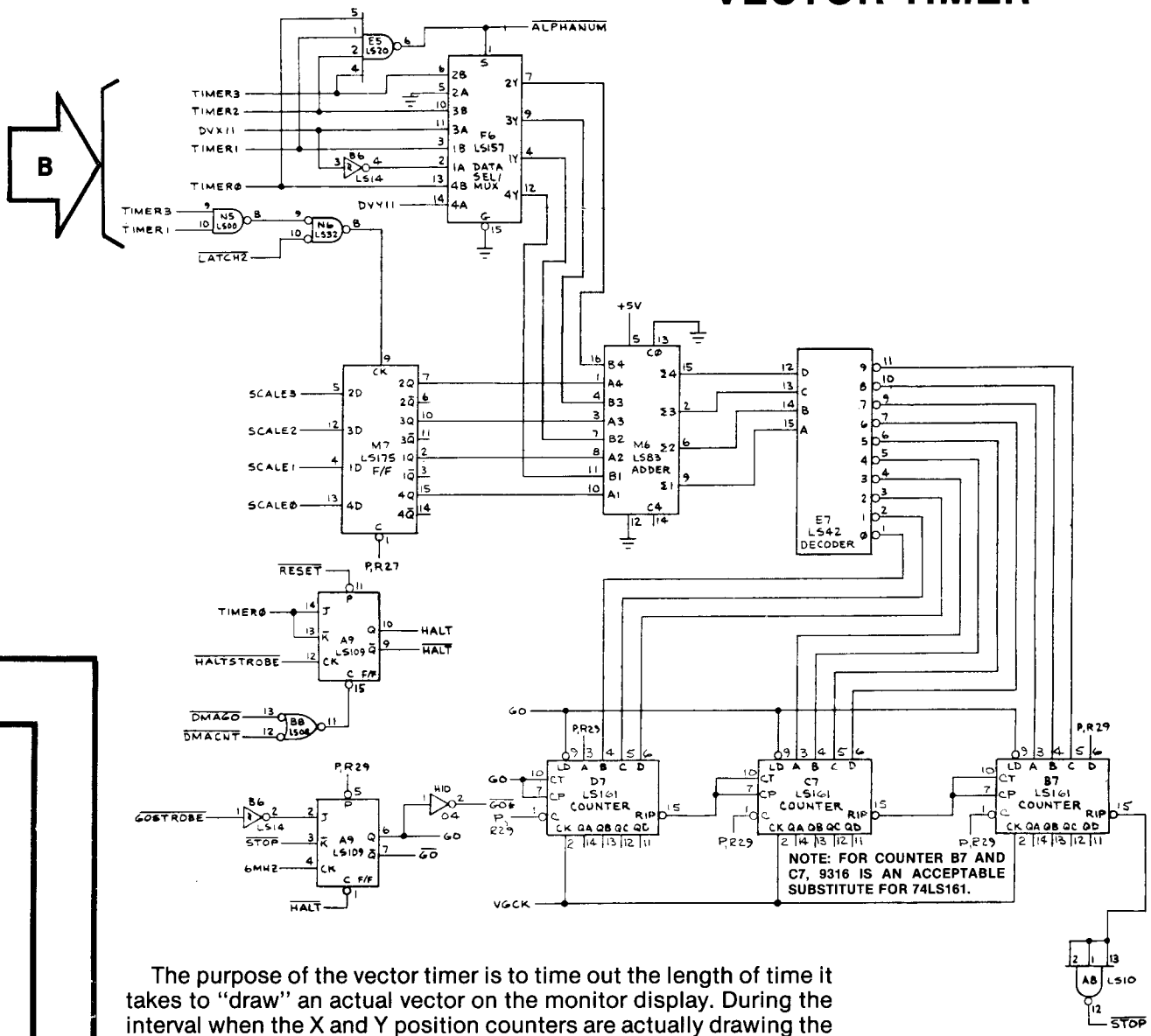
DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different lengths will still be displayed with the same relative beam intensity. DVX10 and 11 are loaded directly into the counters. DVX10 determines whether the counter to control the select input of m

The UNMDACX1 thru UNMDA to-analog converter signals) ar multiplexers and stored at the o edge of the 6 MHz clock (from The DACX1* thru DACX10* sign converters (DACs) in the X vide

The DACX1* thru DACX10* ou ment of the beam on the monito is 0, the center is 512, and the DACX1* thru DACX10* signal beam would go off the right sid the left side of the screen, a "w wraparound, the multiplexers' s high when the count is greater t UNMDACX12 to be output from ing all zeros or all ones, and propriate side on the screen, in

The XVLD and YVLD (X and Y tion counter multiplexers are la the Z axis output, BVLD (beam

VECTOR TIMER



The purpose of the vector timer is to time out the length of time it takes to "draw" an actual vector on the monitor display. During the interval when the X and Y position counters are actually drawing the vector, $\overline{\text{STOP}}$ is high. This prevents the vector generator state machine from advancing to its next state until the vector currently being drawn is completed. As soon as the vector has been drawn, $\overline{\text{STOP}}$ goes low, allowing the state machine to advance to the next state in its intended sequence.

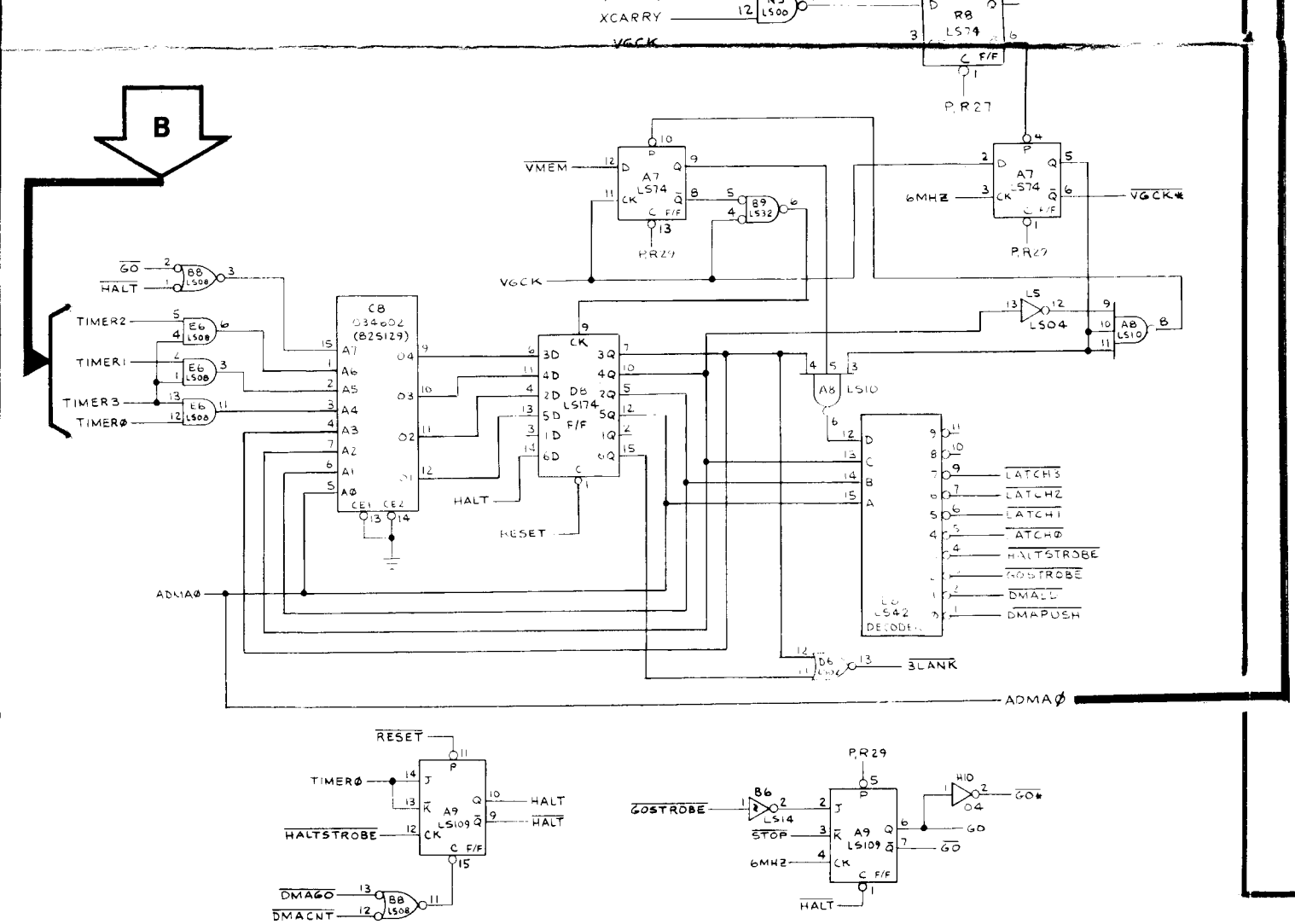
The vector timer consists of multiplexer F6, decoder E7, LATCH M7, ADDER M6, and counters B7, C7, and D7. M7 contains a scale factor which is added in M6 to the four timer signals. If TIMER0 thru TIMER3 inputs are any state but all high, decoder E7 directly decodes the sum and loads the decoded low into one of the counters. When $\overline{\text{GO}}$ goes low, the counters count from the loaded count until the counters all reach their maximum count. This count is a maximum length of 1024. At this time $\overline{\text{STOP}}$ goes low and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, $\overline{\text{ALPHANUM}}$ goes low and data signals DVX11 and DVY11 are decoded by decoder E7. This is added to the scale factor and loaded into the counters.

The X and Y position counters
Therefore, the following descriptior d
counters.

The X position counters contain
down/up counters (C9, D9 and E9), mul
and associated gates (B8 and H10).
counters is a 12-bit binary number th
location of the beam on the monitors
the far left side of the screen and 103
screen. Increasing or decreasing thi
cause the beam to move to the rightor
generator state machine decodes ns
and then is capable of using that dita
these counters in one of two ways.

The state machine can preset thes
ferent number from their previous co
beam to "jump" to a new locationon
taneously, i.e., for drawing a new vec
position than where the previous vect



STATE MACHINE

The state machine is the "master controller" of the vector generator circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator ROM data (via Timer 0-3) and decodes this information to determine how it should use this data: 1) to draw a vector; 2) to move the monitor beam to a new position on the monitor display; 3) to "jump" to a new vector memory address; 4) to return to a previous vector memory address; or 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gates B8 and E6, ROM C8, latch D8, clock circuitry A7, and decoder E8. Four bit input TIMER0 thru TIMER3 is the operation code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input $\overline{GO}$ tells the ROM that the position counters are presently drawing a vector. The $\overline{HALT}$ input to A7 tells the ROM that the vector generator has completed its operations.

During initial power-up of the game, the $\overline{HALT}$ signal is preset low. The microcomputer reads the high HALT signal through its switch input port (buffer M10) on data line DB0. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clocked through latch D8, results in a low $\overline{BLANK}$ to the Z axis output.

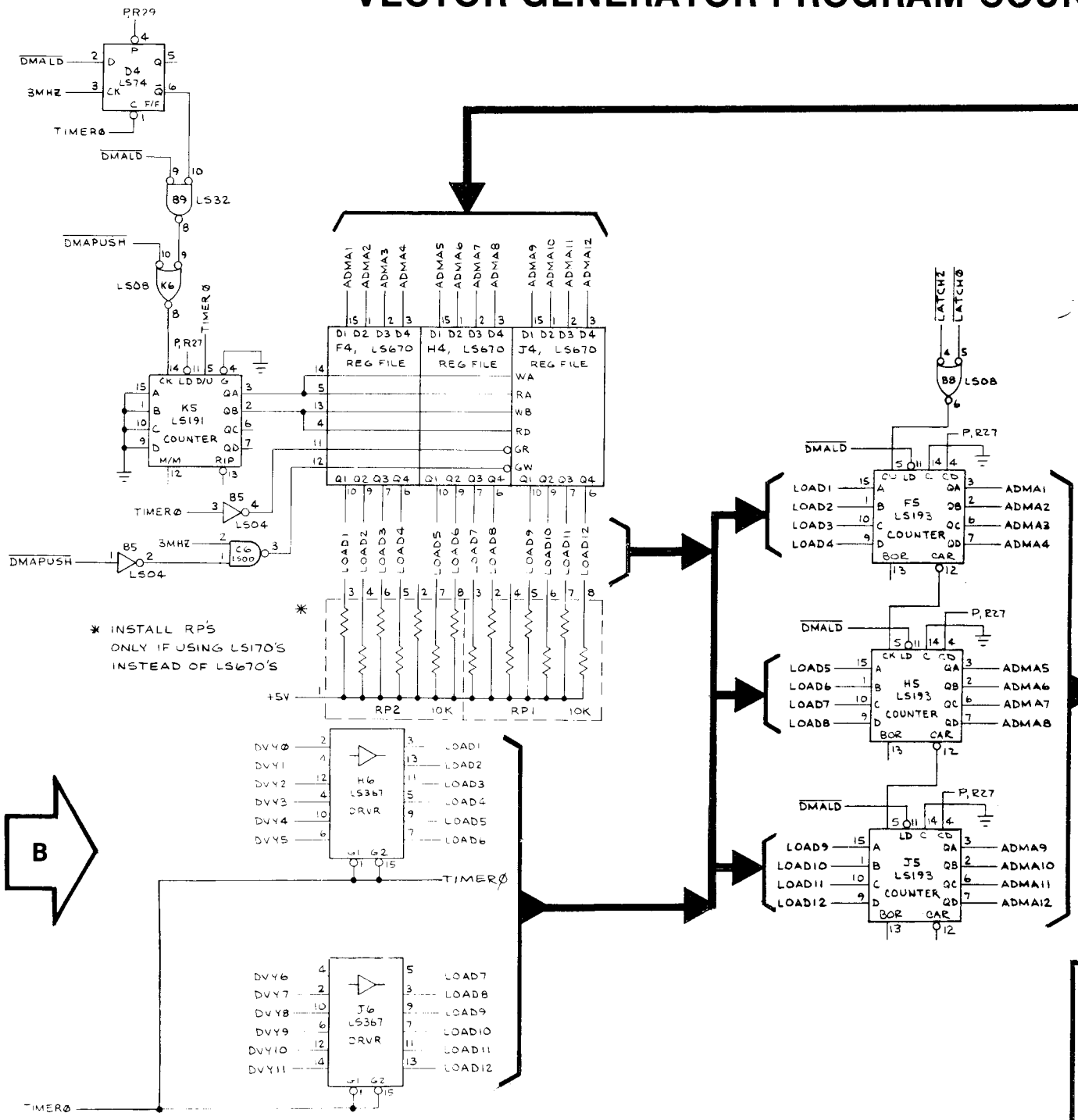
The microcomputer outputs an address that results in a $\overline{DMAGO}$ signal that causes $\overline{HALT}$ to go high, and clears the vector generator data latches. This makes TIMER0 thru TIMER3 signals all low. The state machine now begins executing instructions, starting at vector memory location 0.

When the state machine receives the operation code for a $\overline{HALT}$ instruction, it outputs a low $\overline{HALTSTROBE}$, setting the HALT flip-flop A9, and suspending state machine operation.

The GO signals load and enable the vector timer and the X and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The $\overline{HALT}$ input to GO flip-flop A9 sets the outputs to ensure that the vector timer and position counters are not active when the state machine is halted. When a low $\overline{GOSTROBE}$ is clocked through A9, the vector timer and X and Y position counters begin to operate from the GO, $\overline{GO}$ and $\overline{GO}$* signals. When $\overline{STOP}$ is clocked through A9, the vector timer has reached its maximum count, and $\overline{GO}$ goes high. This means the vector has been drawn.

The VGCK input to the clock circuitry is a buffered 1.5 MHz clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when $\overline{VMEM}$ goes low). Then the clock input to latch D8 goes high and stays high until $\overline{VMEM}$ goes high.

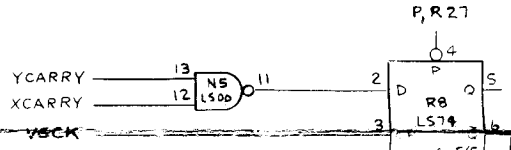
VECTOR GENERATOR PROGRAM COUNTER



Counters F5, H5 and J5 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented one count (to the next sequential address) each time the information at its current address is loaded into data latch 0 or data latch 2.

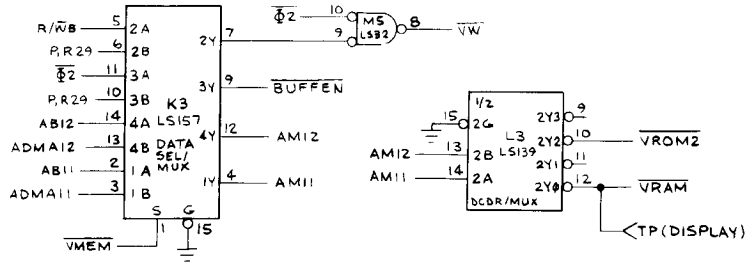
The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F7 and H7 and buffers H6 and J6.

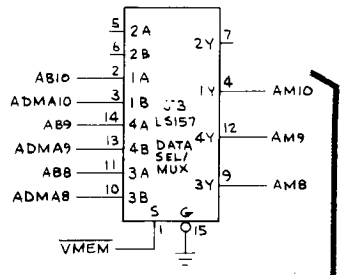
The program counter may also be preset to "return" to a previous address which it had stored in its "stack". The stack consists of register files F4, H4, & J4, and down/up counter K5. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when $\overline{\text{DMAPUSH}}$ is low. Immediately after information is written into the stack, counter K5 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.

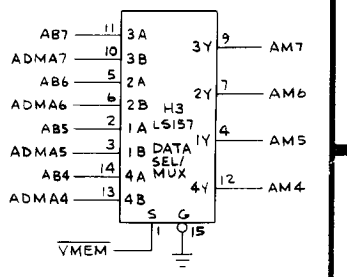


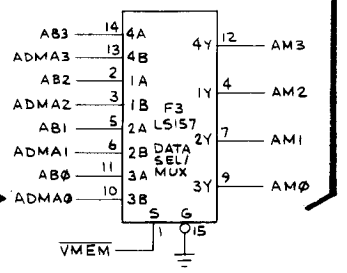
FROM MICROCOMPUTER SHEET 1, SIDE B

VECTOR GENERATOR MEMORY ADDRESS SELECTOR







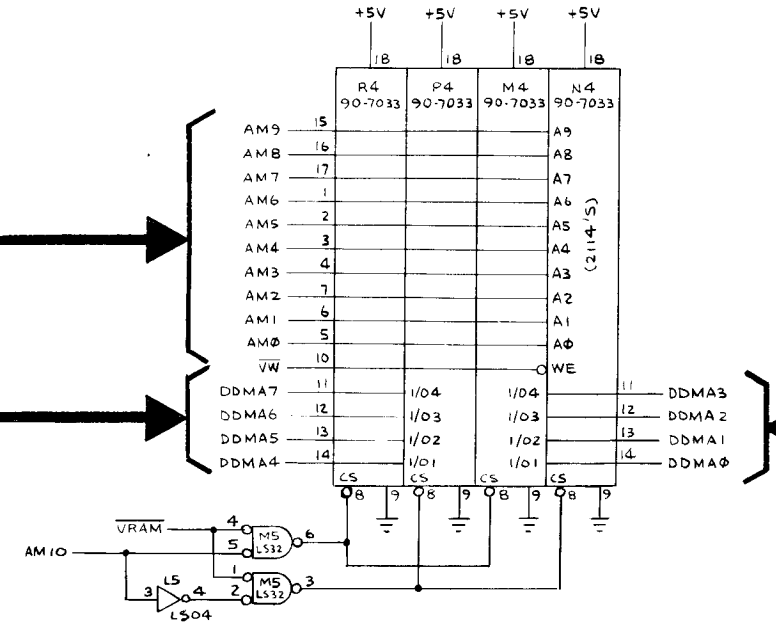


The address selector consists of multiplexers F3, H3, J3 and K3. When $\overline{VMEM}$ is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, $\overline{BUFFEN}$ is from $\overline{\Phi 2}$ and $\overline{VW}$ (vector generator write) is low when $\overline{\Phi 2}$ and $\overline{R/WB}$ are both low. When $\overline{VMEM}$ is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, $\overline{BUFFEN}$ and $\overline{VW}$ are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K3.

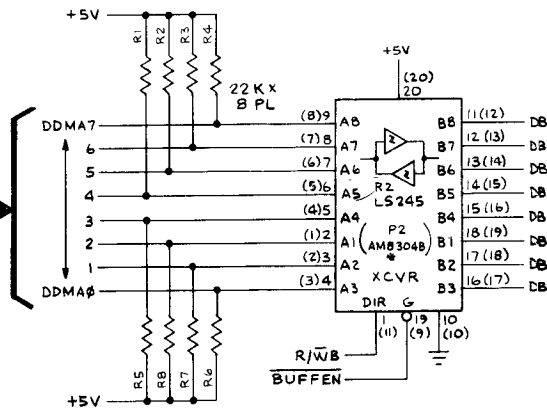
Address decoder L3 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector generator memory.

This address-selecting arrangement allows the game MPU to access the vector generator memory, i.e., write data into the vector generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

ENERATOR RAM

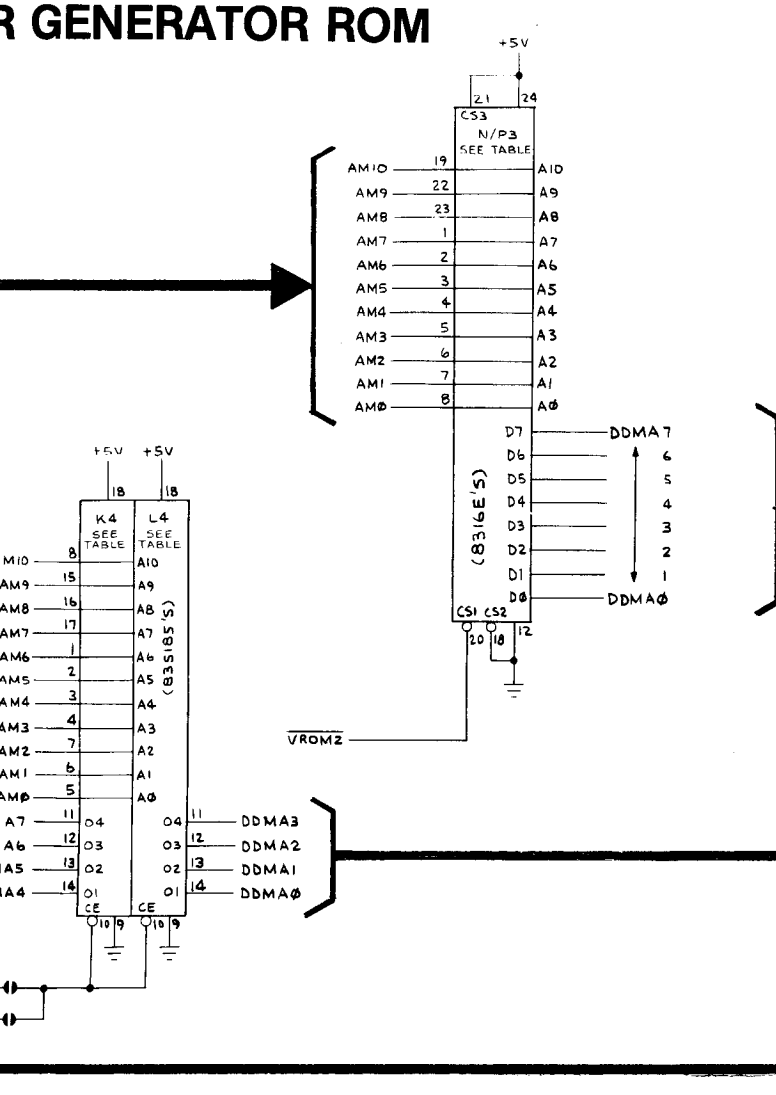


VECTOR GENERATOR DATA BUFFER



* USE PIN NUMBERS IN PAREN-
THESES IF BOARD CONTAINS
AM8304B INSTEAD OF 74LS245

R GENERATOR ROM



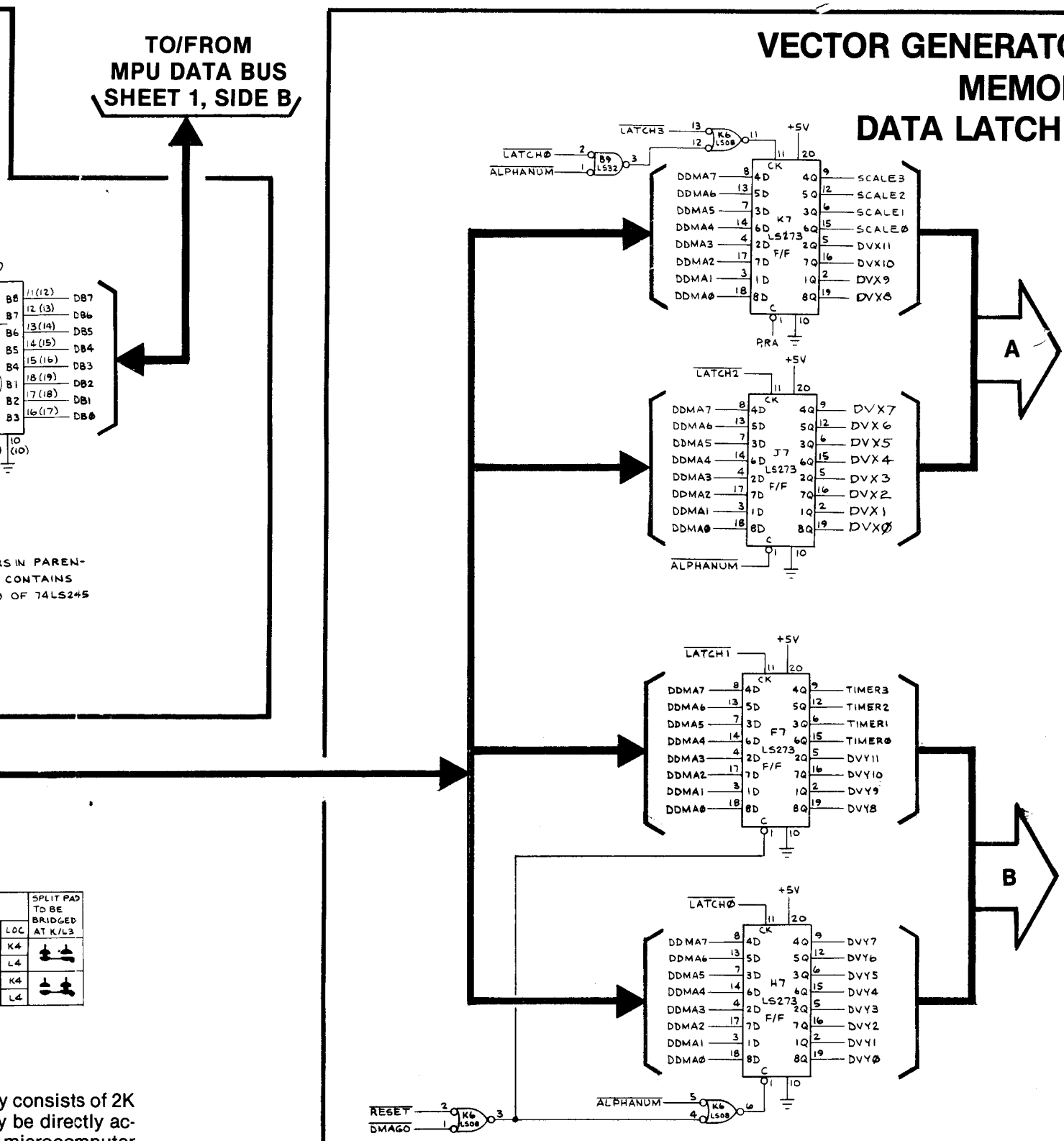
VECTOR MEMORY ROM/PROM SUBSTITUTION				SPLIT PAD TO BE BRIDGED AT K/L3
ROM #	LOC	PROM #	LOC	
035127	N/P3	035129	K4	
		035130	L4	
	R3		K4	
			L4	

The vector generator memory consists o
of RAM and 4K of ROM. It may be directl
cessed by the MPU of the microcomp
through the direct memory access pro
(DMA). Data is written in from the micro
puter thru data buffer R2 when BUFFEN
R/WB are low.

The 2k×8 vector generator prog
memory chip N/P3 may be substituted
two equivalent 1K×8 chips in location K4
L4.

denotes change by indicated re

VECTOR GENERATOR MEMORY DATA LATCHES



y consists of 2K
y be directly ac-
microcomputer
access process
the microcom-
n BUFFEN and

rator program
ubstituted with
location K4 and

The data latches consist of latch 0 (H7), latch 1 (F7), latch 2 (J7), and latch 3 (K7). Inputs DDMA0 thru DDMA7 are the data outputs from the vector generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.

outputs are applied to the pin 6 inputs of current-to-voltage converters C12 and A12.

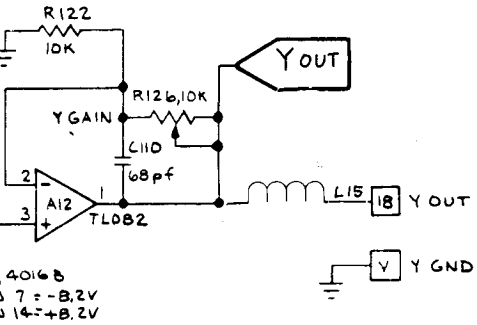
From the current-to-voltage converters, the signal is fed to two sample-and-hold circuits: One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C98 for the X axis, and B12 and C106 for the Y axis. The inverting sample and hold consists of inverter E12, one stage of analog switch D12, and capacitor C119 for the X axis and B/C12, B12 and C118 for the Y axis.

The sample and hold circuits are controlled by SHCON (sample and hold control). SHCON is derived by gating 3 MHz from the microcomputer clock circuitry and VGCK* from the vector generator's state generator. The result of these inputs insures that the non-inverted and inverted analog signals that are applied to the analog switches have sufficiently stabilized before being applied to the sample and hold capacitors.

The output swing of SHCON is −8 to +8 VDC. When SHCON is high, the voltage charges or discharges the sample-and-hold capacitors to the X and Y analog voltage value. The voltages are then applied to the inputs of the second analog switch. These switches select either the non-inverted or inverted X-axis and Y-axis outputs. The outputs are then amplified by the second stages of C12 and A12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor doesn't have field-adjustable X and Y gains, the gains are adjustable by variable resistors R120 and R126.

Z Output

The Z axis video output receives six inputs. BVLD (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (vector line blank), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 thru SCALE3 (grey level shading scale), from the output of the vector generator's data latch, tells the Z axis the grey level shading of the line that is being drawn on the monitor.



When BVLD and BLANK are both high, a high is clocked through shift register K9 that turns transistor Q3 off. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs at the base of transistor Q1 determine Q1's emitter voltage, during the line draw period. The SCALE0 thru SCALE3 resistors R36 thru R39, resistor R35, and resistor R40 result in a range of about +1.0 VDC when all are low and +4.0 VDC when all are high. The emitter of Q1 follows at about +1.7 to 4.7 VDC, while the emitter of transistor Q2 follows at about +1.0 to 4.0 VDC. This output is applied to the Z input of the monitor. Since there are brightness and contrast controls in the monitor, there are no adjustments in this circuit.

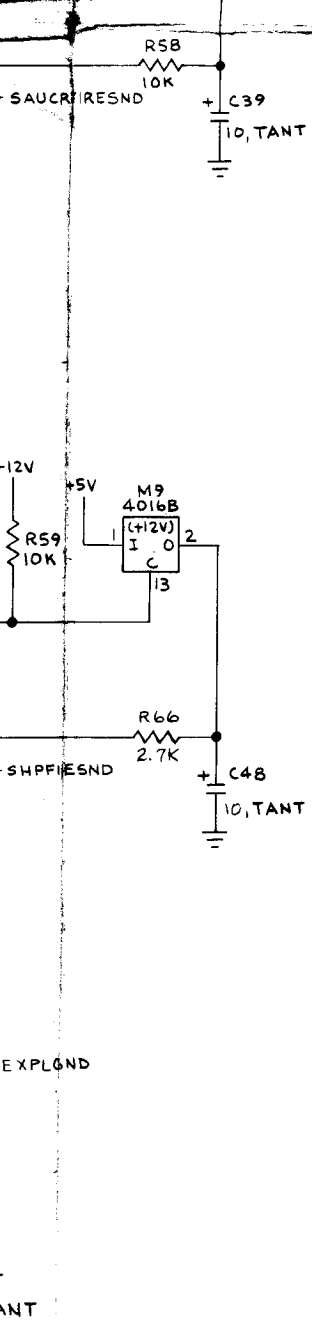
Sheet 2, Side B

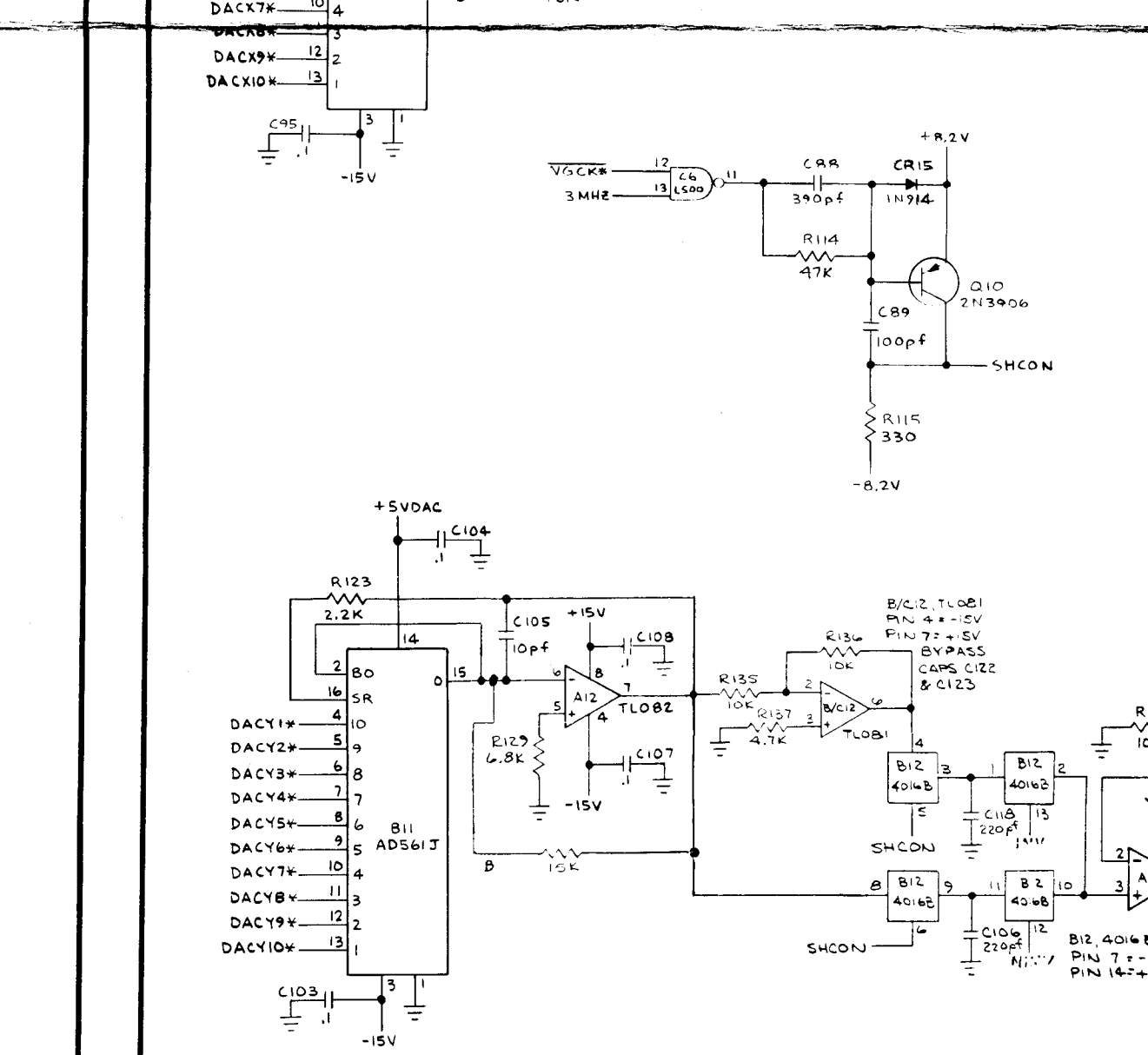
COCKTAIL ASTEROIDS

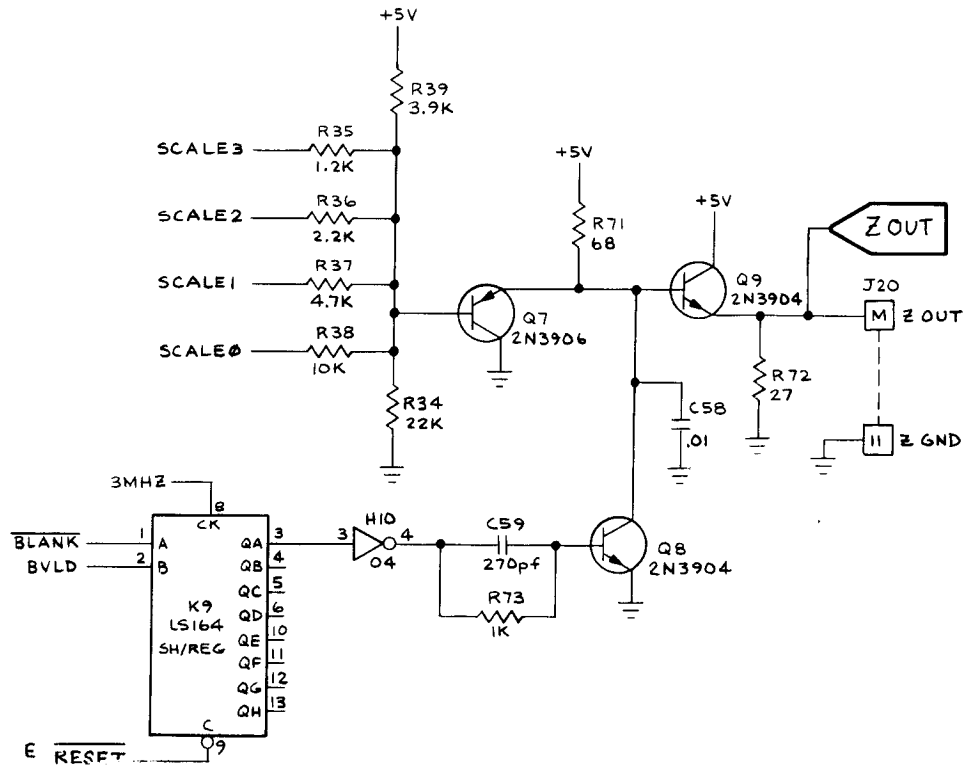
Switch Inputs, Coin Counter, LED and Audio Outputs Section of 034986-XX G

ATARI

A Warner Communications Company



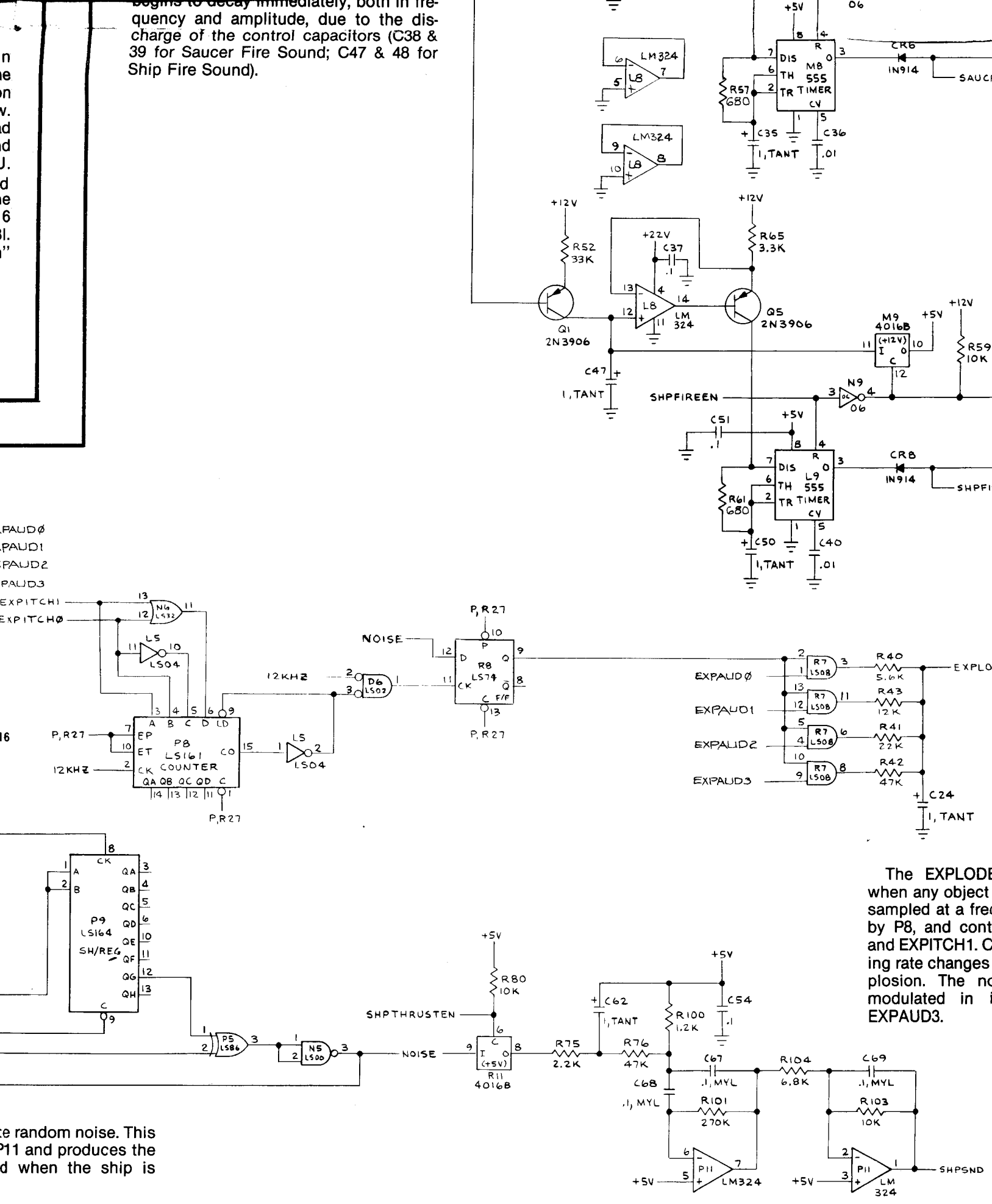




PLOD sound is heard
objecexplodes. Noise is
a frequency determined
control bits EXPITCH0
CH1. hanging the sampl-
angethe pitch of the ex-
he nise is amplitude-
in 37 by EXPAUD0-

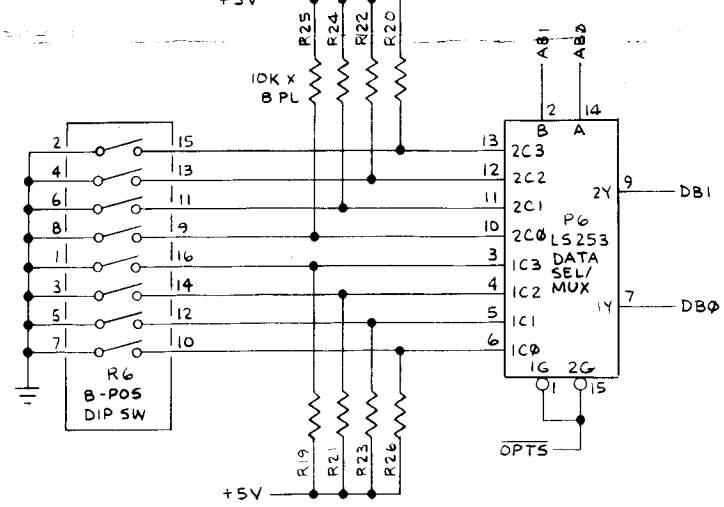
PSND

begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitors (C38 & 39 for Saucer Fire Sound; C47 & 48 for Ship Fire Sound).



The EXPLODE
when any object
sampled at a free
by P8, and cont
and EXPITCH1. C
ing rate changes
plosion. The no
modulated in i
EXPAUD3.

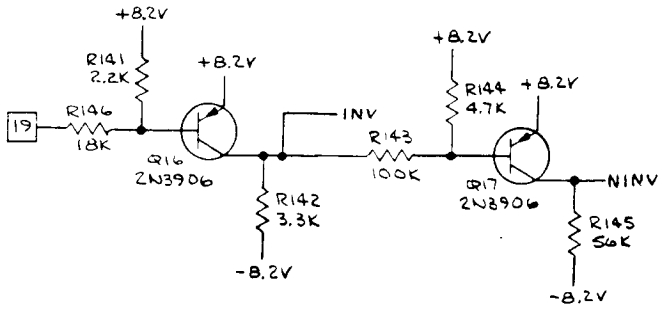
e random noise. This
P11 and produces the
d when the ship is



The game option switches are read by the MPU when $\overline{\text{OPTS}}$ (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 5, and 7 are read on data line DB0 and toggles 2, 4, 6 and 8 are read on DBI. Toggle inputs are "on" when pulled to ground.

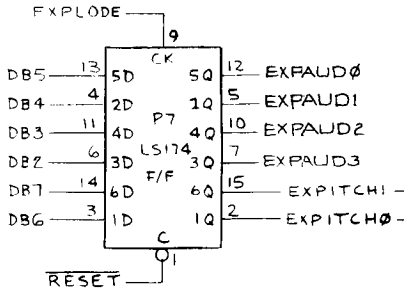
denotes change by indicated revision

VIDEO INVERTER

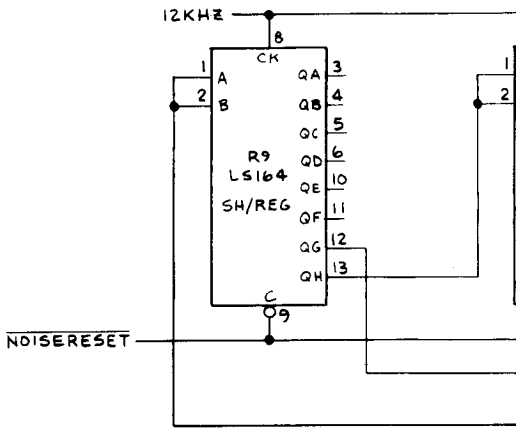


The video inverter circuitry is only used in a cocktail game. In an upright game, pin 19 is unconnected and therefore floats. When pin 19 floats, transistor Q16 is turned off and transistor Q17 is turned on. Therefore, INV is −8.2 VDC and NONINV is about +8.2 VDC. The result is a non-inverted X-axis and Y-axis output.

In a cocktail game, the wiring harness shorts connector J20's output pin 7 input pin 19. When the video of player 1 is being displayed, pins 7 and 19 are +5 VDC. This results in a non-inverted video output. When the video for player 2 is being displayed, pins 7 and 19 are grounded. This causes transistor Q16 to be turned on and Q17 to be turned off. Therefore, INV is +8.2 VDC and NONINV is −8.2 VDC. The result is an inverted X-axis and Y-axis output, causing the monitor's display to be upside down.



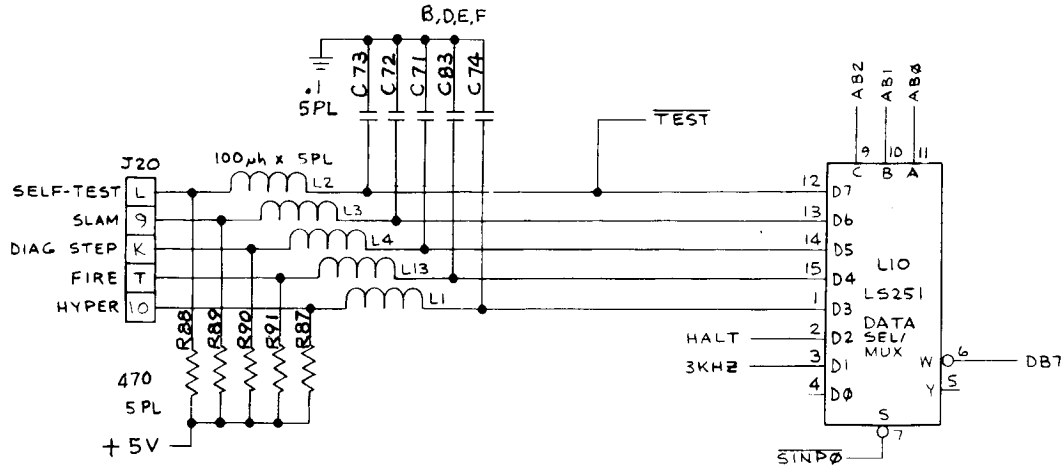
NOTE: FOR COUNTER P8, 9316 IS AN ACCEPTABLE SUBSTITUTE FOR 74LS161.



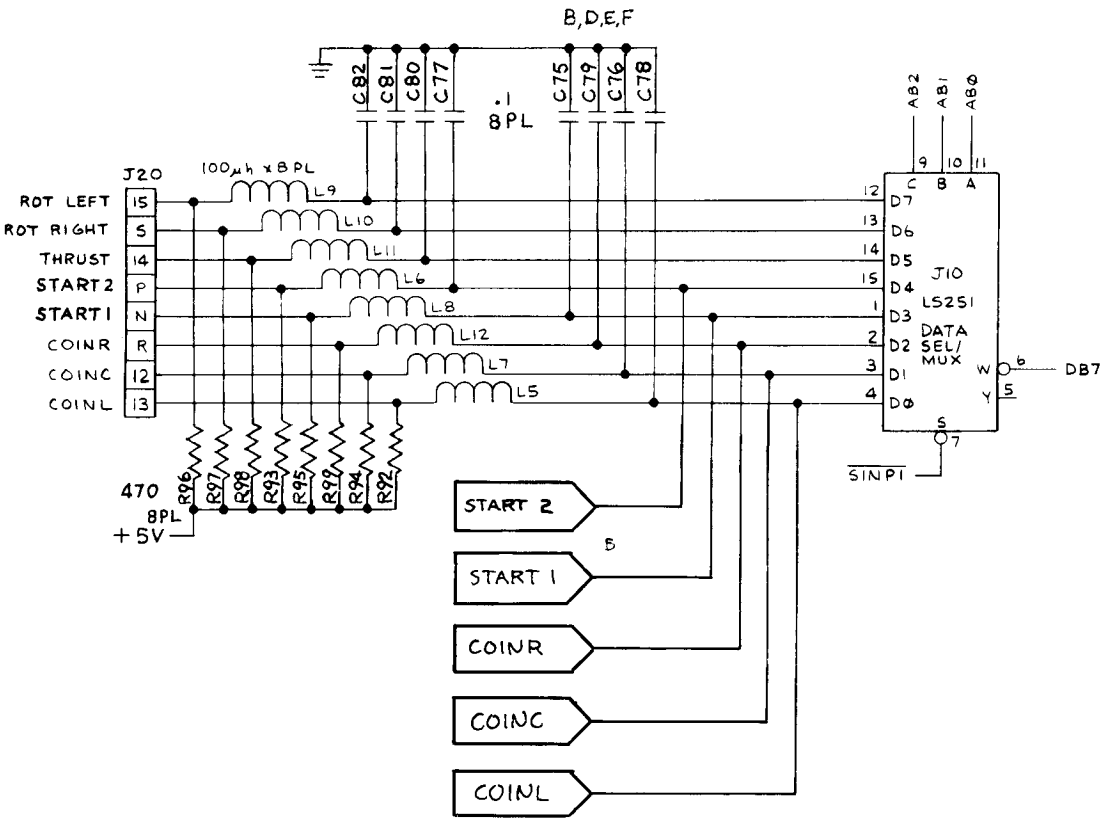
R9 and P9 generate random noise is filtered by P11 and p rumble sound heard when thrusting.

INPUTS

PLAYER INPUT CIRCUITRY

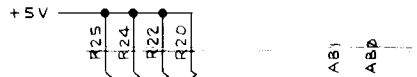


DIAG STEP (diagnostic step), 3 KHz, SELF-TEST SLAM, HALT, FIRE and HYPER inputs are read by the MPU when $\overline{\text{SINP0}}$ (switch input zero enable) is low, Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on DB7. Switch inputs are active when pulled to ground. DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

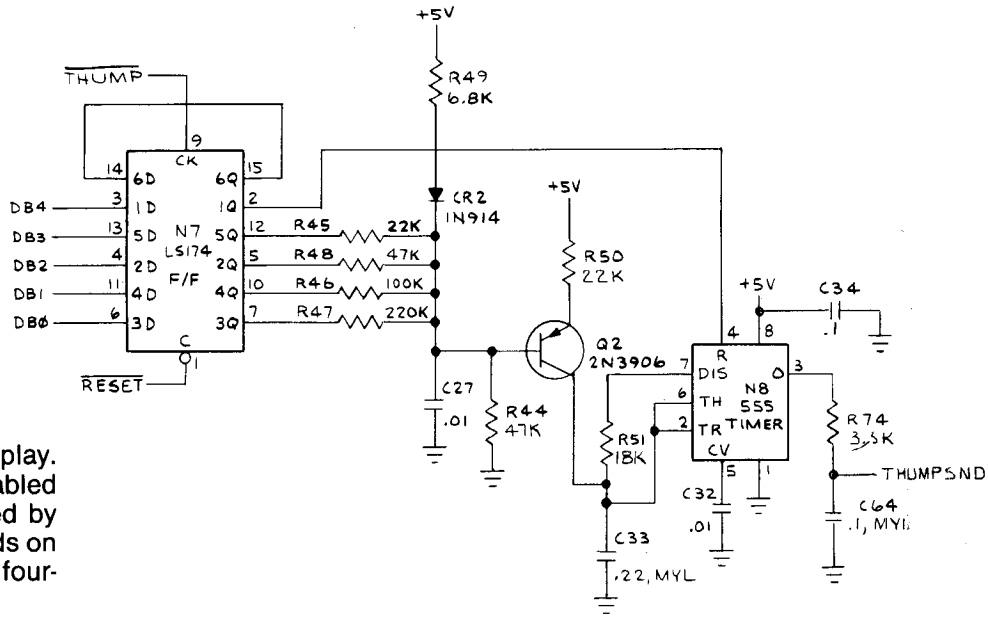


The coin door and some control panel switches are read by the MPU when $\overline{\text{SINP1}}$ (switch input one enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

OPTIONS INPUT CIRCUITRY

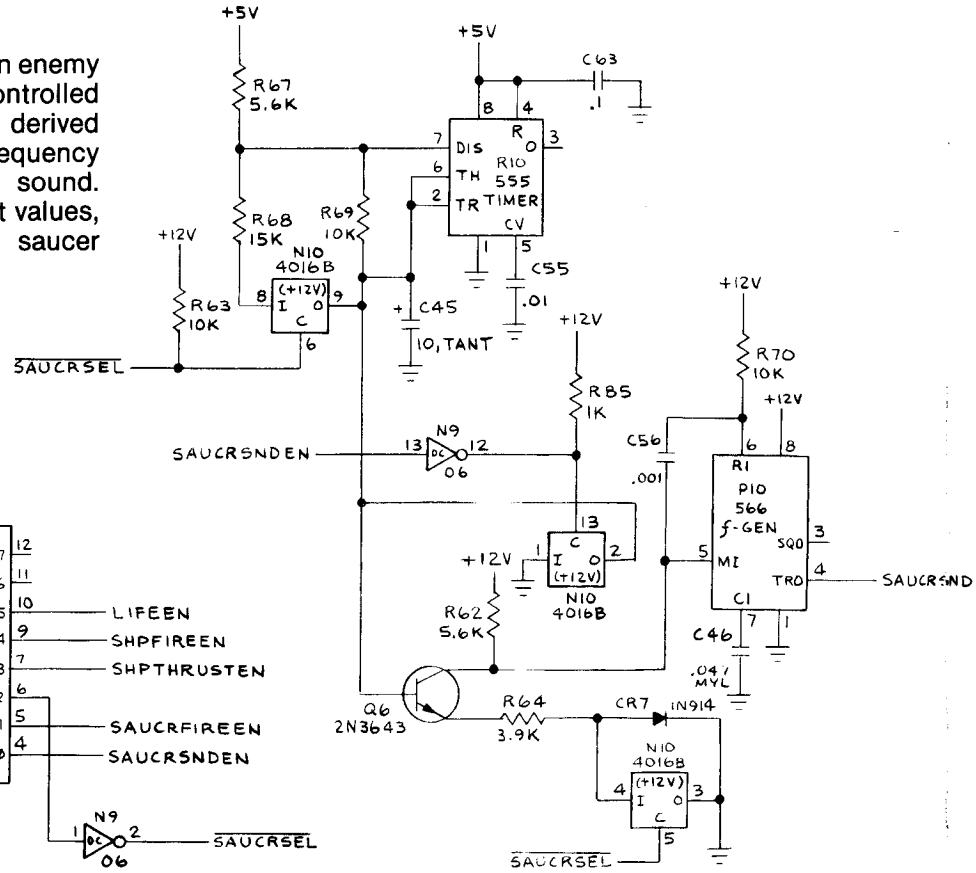


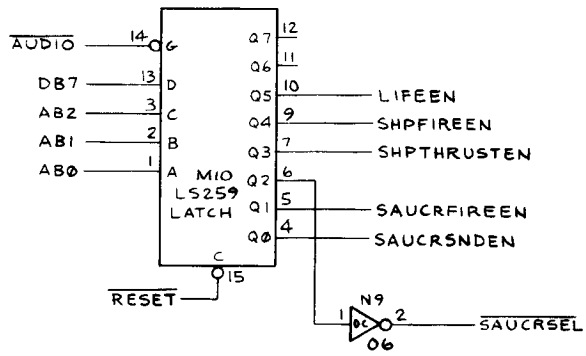
OUTPUTS



The THUMP sound is heard throughout play. The 555 is connected as an oscillator, enabled by N7 pin 2. The frequency is determined by the current coming out of Q2. This depends on its base voltage, which is derived from the four-bit code in N7.

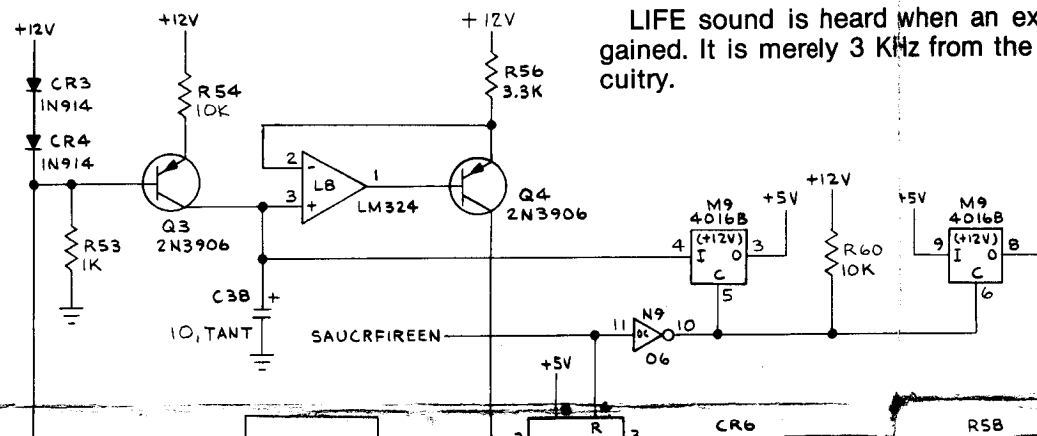
The SAUCER sound is heard when an enemy saucer appears. The 566 is a voltage-controlled oscillator. Its modulating voltage is derived from the 555. The 555 is a low frequency oscillator. The effect is a warbling sound. SAUCRSEL changes some component values, in order to provide for 2 different saucer sounds.





M10 latches control signals to enable different sounds.

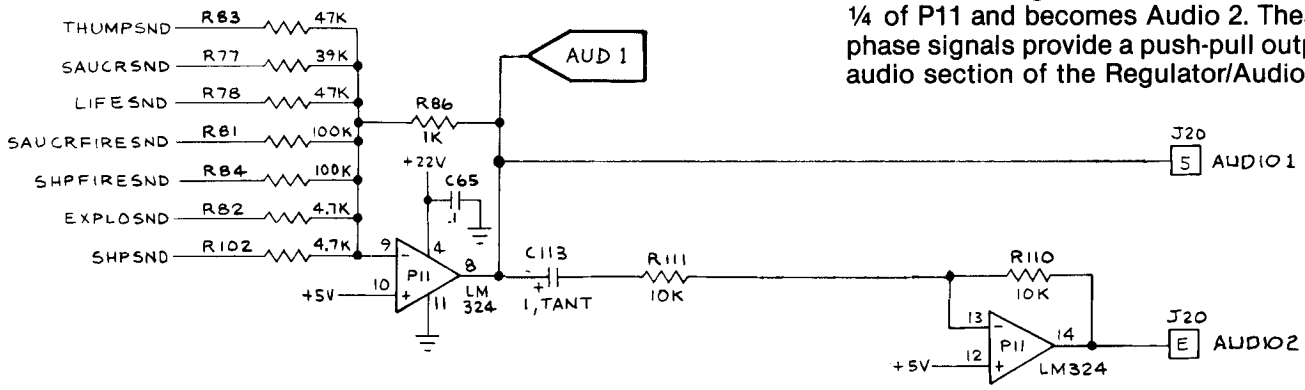
The Fire sounds for the Saucer and the Space Ships are generated by two identical circuits. Each contain a 555 operating as a voltage-controlled oscillator. The Saucer Firesound is initiated by SAUCRFIREEN, and the Space Ship Fire sound is initiated by SHPFIREEN. Each of the 555s is configured in such a way that when they are enabled, they output a signal of a specific frequency and amplitude. This signal begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitors (C38 &



LIFE sound is heard when an ex
gained. It is merely 3 KHz from the
cuitry.

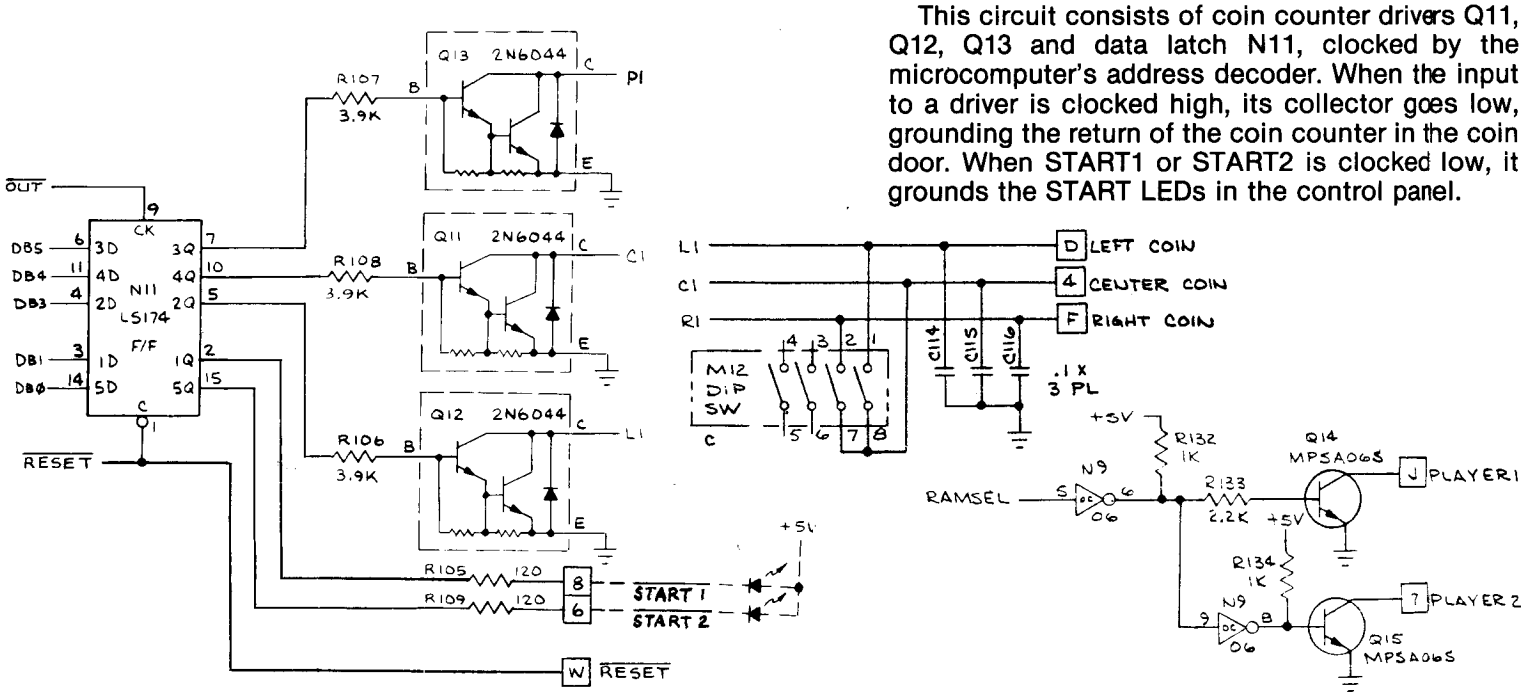
AUDIO OUTPUT

All sounds are mixed in ¼ of P11. This is Audio 1. The signal is then inverted by another ¼ of P11 and becomes Audio 2. These out-of-phase signals provide a push-pull output to the audio section of the Regulator/Audio PCB.



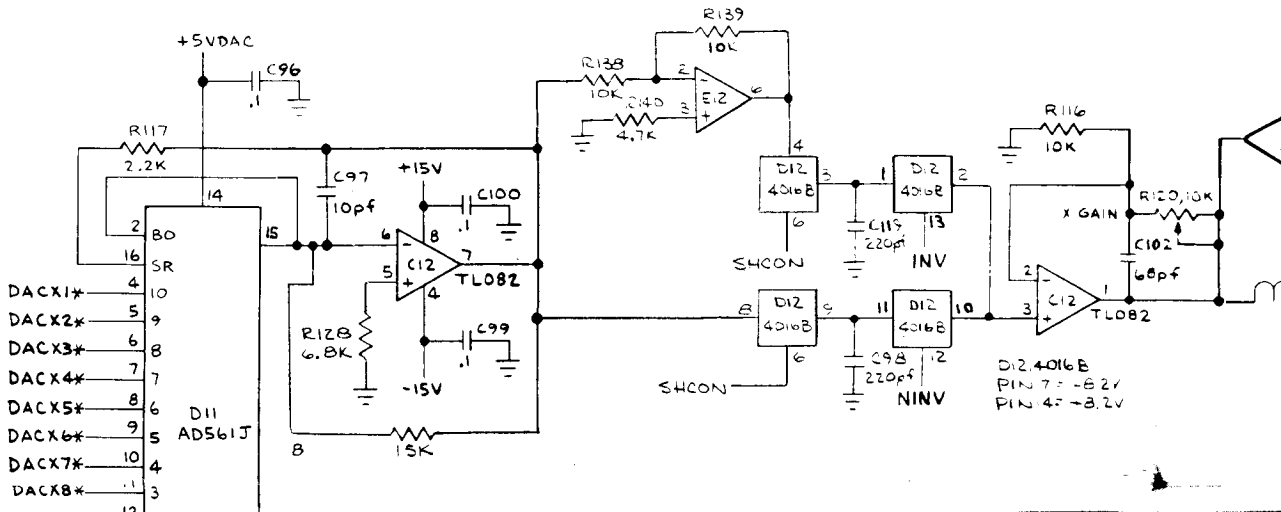
LAMP, LED, AND COIN COUNTER OUTPUT

This circuit consists of coin counter drivers Q11, Q12, Q13 and data latch N11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door. When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.



extra life is
he clock cir-

VIDEO OUTPUTS

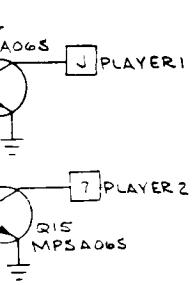


f P11. This is
ed by another
These out-of-
output to the
udio PCB.

ıo 1

ɔ102

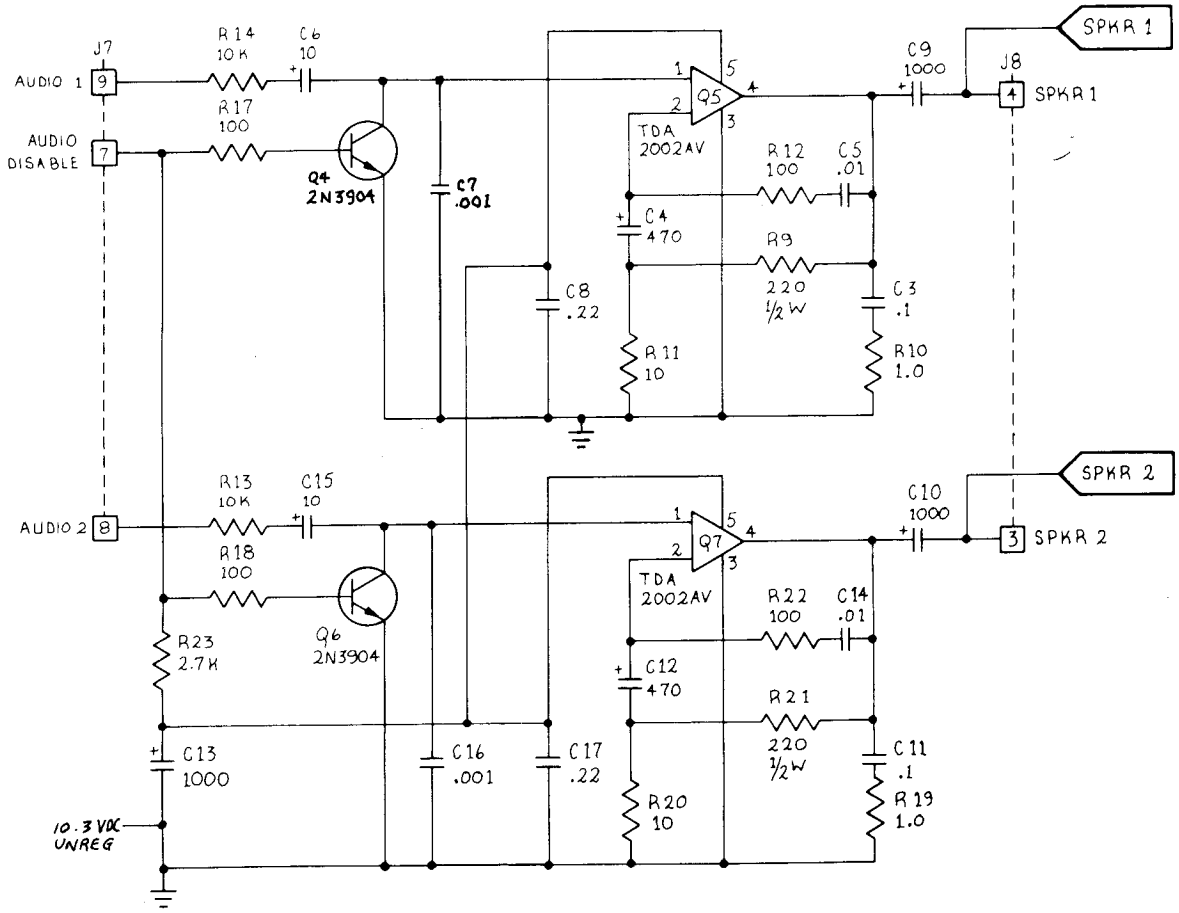
ter drivers Q11,
locked by the
When the input
ector goes low,
nter in the coin
clocked low, it
ntrol panel.



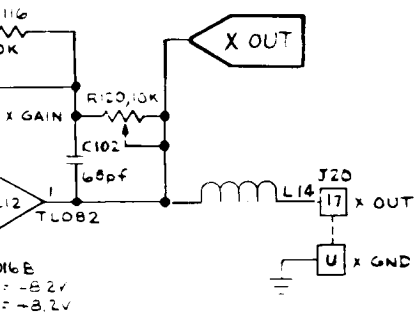
PART OF REGULATOR/AUDIO PCB

NOTE:
AUDIO AMPLIFIER IS PART OF REGULATOR/AUDIO PCB AND IS REPEATED ON SHEET 1, SIDE A.

Audio inputs AUDIO 1 and AUDIO 2 receive out of phase signals for push-pull operation. AUDIO DISABLE is permanently grounded for continuous audio amplification.



denotes a test point



The video output circuit consists of three individual circuits; X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and holds, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (D11 and B11) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, where 0 is at the far left of the monitor screen, 512 is at the center, and 1023 is at the far right. For the non-inverted Y axis, the numbers range from 128 to 996, where 128 is at the bottom of the monitor screen, 512 is at the center, and 996 is at the top. When the X axis and Y axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary number inputs to current outputs. The DACs' current outputs are applied to the pin 6 inputs of current-to-voltage converters C12 and A12.

From the current-to-voltage converters, the signal is fed to two sample-and-hold cir-