ASTEROIDS DELUXE

SIGNATURE ANALYSIS

GUIDE

Introduction

This guide is intended as an aid to troubleshooting the Asteroids Deluxe video game PCB. The Signature Analyzer used to produce this guide was an HP5004a. If it is found that the signatures hold up for other makes/models of Signature Analyzers then please let me know and I can add some kind of compatibility list to the document. Suggestions of any kind to improve this document are always welcome.

To get the most out of the guide you'll need

Signature Analyzer (HP5004a)
Schematics for Asteroids Deluxe
6502 NOP card (See the separate document 6502NOP for instructions on how to build your own NOP card)
IC Clips
Some jumper wires (3 or 4 should be sufficient)

The scope of the guide is limited in that it will not enable you to fault find the entire PCB. It should, however, be good for the following sections of the PCB:

Address Bus Buffers, Address Decoding Circuitry, Clock Circuit, Program ROMs and Data Buffer, Vector Generator Address Selector, Vector Generator RAM Select, Vector Generator ROMs and the Vector Generator Data Buffer.

The Clock Circuit test is very limited. The reason being is that I much prefer to check the clock chain with a scope. If you want to figure out the signatures for the Clock Circuit then pass on the information and I'll include it in the document. If you want a detailed description of these sections (and more) please refer to the Asteroids Deluxe schematic / drawing package.

Using The Guide

For those of you who have used Atari Signature Analysis guides before then this should look familiar and there's probably no need to read through this section. For the rest of you, here's a quick run down. Every section should start with the settings for the Analyzer, something like this

A. SA Settings for xxxxx Test

Probe	Trigger	IC Pin	Test Pt.
Start	+ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	$\phi 2$

The probe column refers to either the Start, Stop or Clock probes from the Signature Analyzer.

The trigger column sets up the Start/Stop/Clock buttons on the front of the Analyzer. I have used –ve to indicate the negative going edge of the pulse (or the falling edge).
I have used +ve to indicate the positive going edge of the pulse (or the rising edge).
The IC Pin column refers to the point where the appropriate probe should be attached.
The Test Pt. column refers to an equivalent Test Point on the boards where the probe may be attached.

For example, in the example above the Start probe should be connected to pin 25 of IC C2. The Start button on the front of the Analyzer should be in the fully out position to indicate a positive going edge. Similarly, the Stop probe should be connected to the same IC/Pin as the Start probe but the Stop button on the Analyzer should be pressed in to indicate a negative going edge.

The section immediately following the set up procedure contains the signatures for that part of the test. The same structure for the Set Up was employed as explained below.

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
C1-20	+5V	0003
C1-9	AB0	UUUU
C1-12	AB1	FFFF

Here, with the Analyzer probe on pin 20 of IC C1 you should get a reading of 0003. On pin 9 of IC C1 you should get a reading of UUUU. And so on.

A signature denoted by an (*) indicates that signature may be unstable. Try taking the signature with a 1Kohm resistor connected between the probe tip and +5V.

Down To Business

One of the things I like about this testing method is that you don't need to have the PCB in the cabinet. If you prefer to work in the back of the cabinet then that's fine. If you have a bench/test area with a +5V PSU (as I'm sure most of you have), then you can sit comfortably at the bench. Simply connect Ground (pins 1 and 22 on the edge connector) and +5V (pins 2 and 21 on the edge connector) to the PCB and you're ready to start.

Just set up the Analyzer as indicated and start probing for those signatures. Always remember to have the Watchdog disabled as this will lead to permanently unstable signatures.

What To Do When You Find An Incorrect Signature

If you find a signature that doesn't match the guide, check your set up first. If your set up is OK then you'll need to trace the fault. Rather than having a long winded ramble from me it would be better to look at the following link on Al Kossow's page. If you haven't already had a look at his site then I'd definitely recommend having a look as it's a bit of a gold mine.

http://www.spies.com/arcade/TE/SigAnalNotes.pdf

After you've had a look through the document then you should know enough to start tracing the fault. It should also give you a bit more information on Signature Analysis in general.

Some Common Faults

The two most common faults I've come across are bad sockets and shorted traces. During the Signature Analysis the bad socket problem is highlighted by the fact that the signatures are unstable. You may get some stable and some not. When you get unstable signatures whilst doing the ROM tests it does not necessarily indicate a bad ROM. Reseating the ROM or replacing the socket is usually a good place to start. The problem of shorted traces is usually down to something being dragged across the board. Sometimes they can be quite hard to see but Signature Analysis shows it up quite good.

Disclaimer

If you toast yourself, your house, your dog, your family or more importantly your video game, then it's not my fault. You use the information contained in this guide at your own risk. Good luck.

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** Tie the Watchdog Disable test point to ground **

1. Address Lines

A. SA Settings for Address Buffer Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	ϕ2

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
C1-20	+5V	0003
C1-9	AB0	UUUU
C1-12	AB1	FFFF
C1-7	AB2	8484
C1-14	AB3	P763
C1-5	AB4	1U5P
C1-16	AB5	0356
C1-3	AB6	U759
C1-18	AB7	6F9A
B1-18	AB8	7791
B1-14	AB9	6321
B1-9	AB10	37C5
B1-5	AB11	6U28
B1-7	AB12	4FCA
C2-23	A13	4868
C2-24	A14	9UP1
C2-25	A15	0001

2. Address Decoding

A. SA Settings for Address Decoder Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	ϕ2

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
E3-4	SINP0	AF76
E3-5	SINP1	6913
E3-6	OPTS	13HP
E3-9	PMEM	3282
E3-10	VMEM	AH63
E3-11		7APA
E3-12	ZPAGE	P508
D5-10	PKYDCD	3H01
C5-8		3H02
L2-4	PROM0	P933
L2-5	PROM1	UH4P
L2-6	PROM2	A04H
L2-7	PROM3	86C1

C. SA Settings for Address Decoder Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C3-14	6MHz

** Tie R/W test point to ground **

D. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
D5-14	+5V	00UP

D5-4		0066 **(*)**
E4-8		7U7C
L5-1	DMAGO	383U
L5-2	EAADDRL	P759
L5-3	WDCLR	90P8
L5-4	EXPLODE	UA0P
L5-5		A43F
L5-6	EACONTROL	U5FA
L5-7	AUDIO	81F6
L5-9	NOISERESET	1A35
B8-13		00UP
B8-12		A43F
B8-11	DMARESET	A43F

** Remove jumper from R/W test point **

3..Watchdog Circuit

A. SA Settings for Watchdog Circuit Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	ϕ2

** Tie L5-12 to ground **

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
C5-14	+5V	0003
C5-6		752C
D4-6		0398
D4-8		0000

** Remove jumper from L5-12 **

4..Clock Circuit

A. SA Settings for Clock Circuit Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	ϕ2

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
B3-6		763H
B3-8	3KHz	8A4U
B3-10	12KHz	9720

5 ROM And Data Lines

A. SA Settings for ROM0 Test (D1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-4	
Stop	+ve	L2-4	
Clock	-ve	C2-39	ϕ2

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
D1-24	+5V	826P
D1-9	DB0	4869
D1-10	DB1	995C
D1-11	DB2	F0AH
D1-13	DB3	UF20
D1-14	DB4	A17H
D1-15	DB5	232H
D1-16	DB6	4590
D1-17	DB7	99P1

C. SA Settings for ROM1 Test (E/F1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-5	
Stop	+ve	L2-5	
Clock	-ve	C2-39	ϕ2

D. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
E/F1-9	DB0	UOF3
E/F1-10	DB1	0UCU
E/F1-11	DB2	0CA5
E/F1-13	DB3	A391
E/F1-14	DB4	7F79
E/F1-15	DB5	U77P
E/F1-16	DB6	H494
E/F1-17	DB7	052H

E. SA Settings for ROM2 Test (F/H1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-6	
Stop	+ve	L2-6	
Clock	-ve	C2-39	ϕ2

F. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
F/H1-9	DB0	P65C
F/H1-10	DB1	6FH0
F/H1-11	DB2	7C88
F/H1-13	DB3	PC19
F/H1-14	DB4	94HP
F/H1-15	DB5	CP77
F/H1-16	DB6	4AF2
F/H1-17	DB7	7P08

G. SA Settings for ROM3 Test (J1)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-7	
Stop	+ve	L2-7	
Clock	-ve	C2-39	ϕ2

H. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
J1-9	DB0	373U
J1-10	DB1	U96F
J1-11	DB2	76U1
J1-13	DB3	91PP
J1-14	DB4	9P50
J1-15	DB5	A126
J1-16	DB6	10A0
J1-17	DB7	F002

6. Data Buffer

A. SA Settings for data buffer test.

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-7	
Stop	+ve	L2-7	
Clock	-ve	C2-39	ϕ2

B. Signatures

Logic Probe On IC/Pin	Signal Name	Signature
E2-18 (19)	D0	373U
E2-17 (18)	D1	U96F
E2-16 (17)	D2	76U1
E2-15 (16)	D3	91PP
E2-14 (15)	D4	9P50
E2-13 (14)	D5	A126
E2-12 (13)	D6	10A0
E2-11 (12)	D7	F002

** The numbers in brackets are the pin assignments when an AM8304B is used as opposed to a 74LS245 **

7. Vector Generator Address Selector

A. SA Settings for VG Address Sel Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	ϕ2

** Tie K2-1 to ground **

B Signatures

Logic Probe On IC/Pin	Signal Name	Signature
K2-1	+5V	0003
K2-4	AM11	6U28
K2-12	AM12	4FCA
L2-10	VROM2	F501
L2-11	VROM1	P693
L2-12	VRAM	AA2A
F2-9	AM0	UUUU
F2-7	AM1	FFFF
F2-4	AM2	8484
F2-12	AM3	P763
H2-12	AM4	1U5P
H2-4	AM5	0356
H2-7	AM6	U759
H2-9	AM7	6F9A
J2-9	AM8	7791
J2-12	AM9	6321
J2-4	AM10	37C5

8. Vector Generator RAM

A. SA Settings for VG RAM Test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	C2-25	
Stop	-ve	C2-25	
Clock	-ve	C2-39	ϕ2

** Tie K2-1 to ground **

B Signatures

Logic Probe On IC/Pin	Signal Name	Signature
M4-3		98H1
M4-6		32U8
L4-4		37C6

9. Vector Generator ROM

A. SA Settings for VG ROM1 Test (R2)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-11	
Stop	+ve	L2-11	
Clock	-ve	C2-39	ϕ2

** Tie K2-1 to ground **

B Signatures

Logic Probe On IC/Pin	Signal Name	Signature
R2-24	+5V	826P
R2-9	DDMA0	A13F
R2-10	DDMA1	37H3
R2-11	DDMA2	9F59
R2-13	DDMA3	69HU
R2-14	DDMA4	9277
R2-15	DDMA5	5530

R2-16	DDMA6	725P
R2-17	DDMA7	2604

C. SA Settings for ROM2 Test (N/P2)

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-10	
Stop	+ve	L2-10	
Clock	-ve	C2-39	ϕ2

** Tie K2-1 to ground **

D Signatures

Logic Probe On IC/Pin	Signal Name	Signature
N/P2-9	DDMA0	6334
N/P2-10	DDMA1	2AH5
N/P2-11	DDMA2	3431
N/P2-13	DDMA3	F67C
N/P2-14	DDMA4	5H7C
N/P2-15	DDMA5	7FFH
N/P2-16	DDMA6	88U2
N/P2-17	DDMA7	A433

10. Vector Generator Data Buffer

A. SA Settings for VG Data Buffer test

Probe	Trigger	IC Pin	Test Pt.
Start	-ve	L2-10	
Stop	+ve	L2-10	
Clock	-ve	C2-39	ϕ2

B Signatures

Logic Probe On IC/Pin	Signal Name	Signature
P1-18 (19)	DB0	6334
P1-17 (18)	DB1	2AH5
P1-16 (17)	DB2	3431
P1-15 (16)	DB3	F67C
P1-14 (15)	DB4	5H7C
P1-13 (14)	DB5	7FFH
P1-12 (13)	DB6	88U2
P1-11 (12)	DB7	A433

* The numbers in brackets are the pin assignments when an AM8304B is used as opposed to a 74LS245 *