

Drawing Package Supplement

to

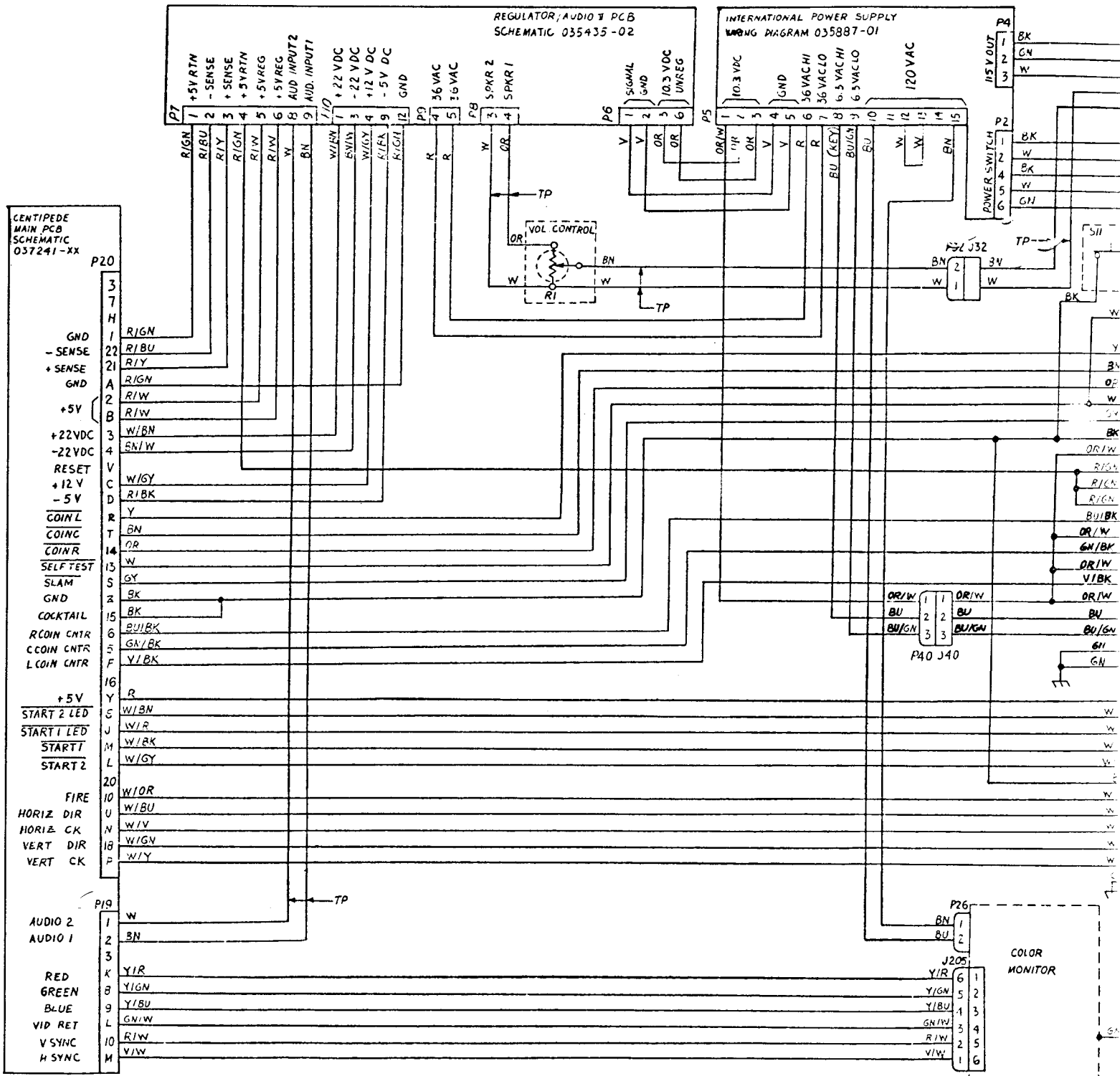
Centipede™

Operation, Maintenance and Service Manual

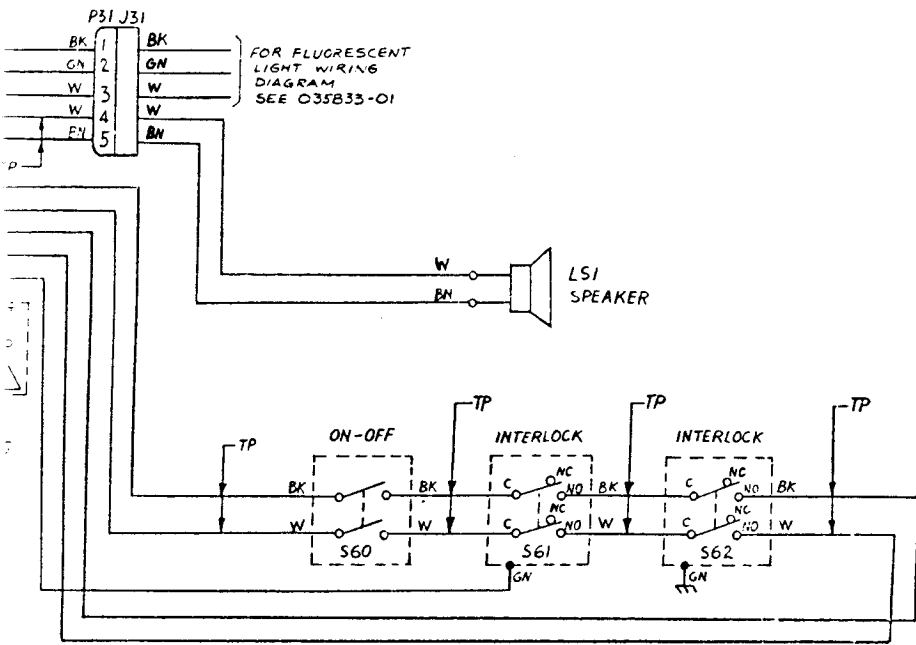
Contents of this Drawing Package

Game Coin Door and Power Supply Wiring Diagram	Sheet 1, Side A
Microprocessor, Signature Analysis Procedure, Sync Generator, CAT Box™, and Power Inputs	Sheet 1, Side B
Playfield Address Selector, Playfield Memory and Playfield Code Multiplexer	Sheet 2, Side A
Coin Door Inputs, Switch Inputs, Video Outputs and Trak Ball™ Circuitry	Sheet 2, Side B

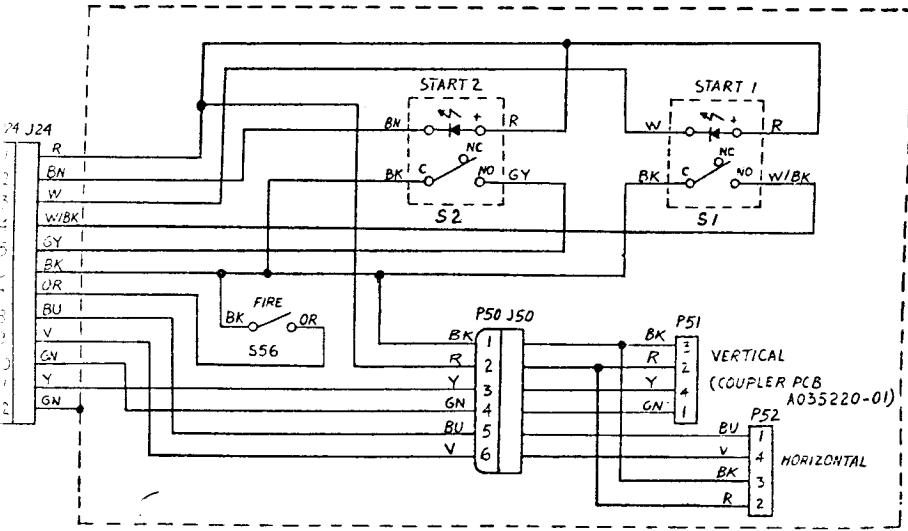
Centipede Wiring Diagram (037432-01 A)



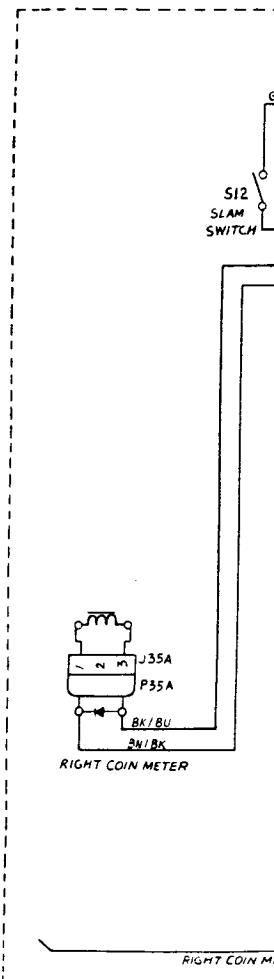
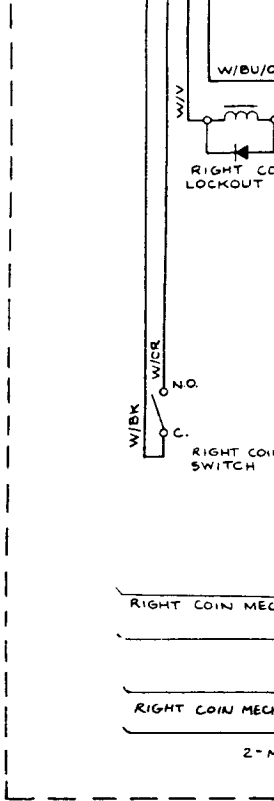
⚠ USE WITH COIN DOORS NOT EQUIPPED WITH TEST SWITCH.

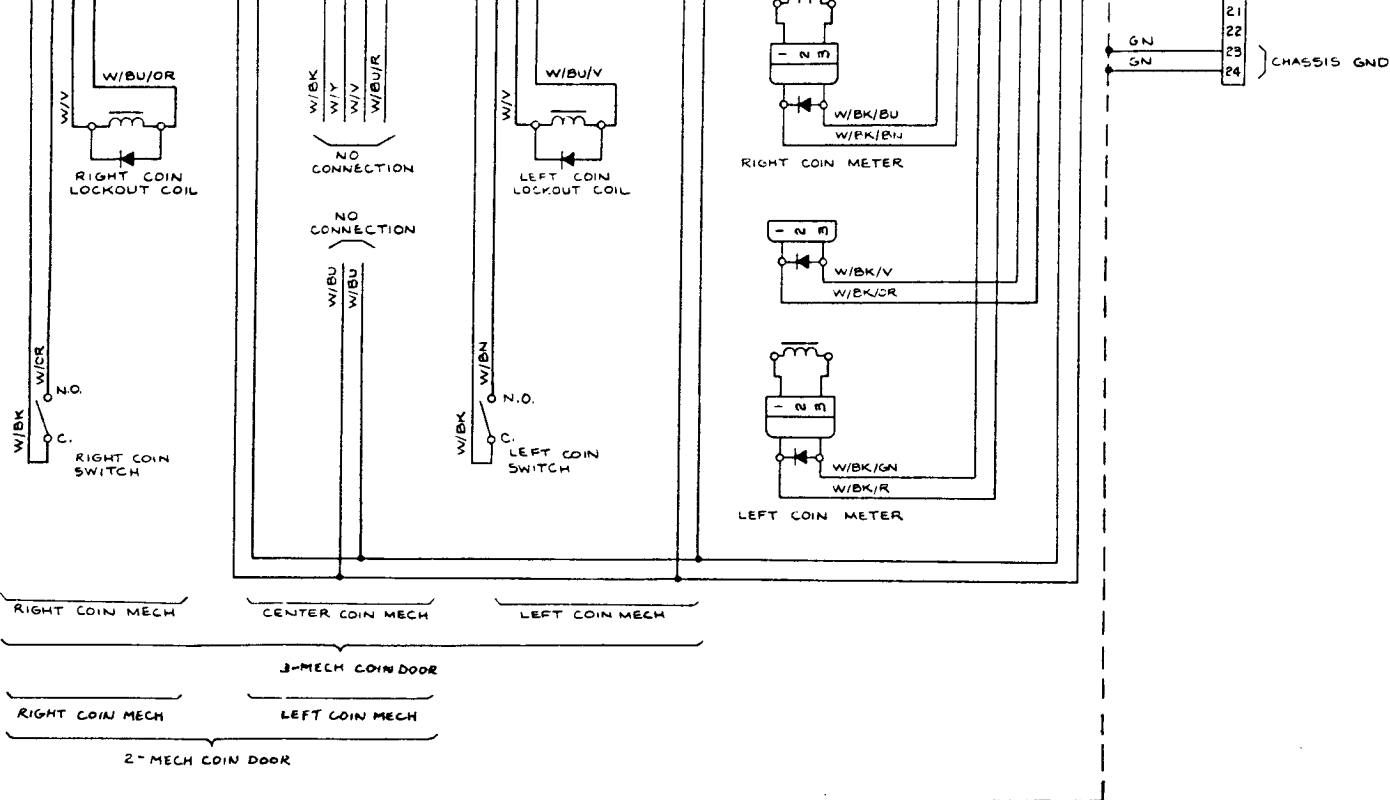


FOR COIN DOOR SCHEMATIC SEE O36B35-01

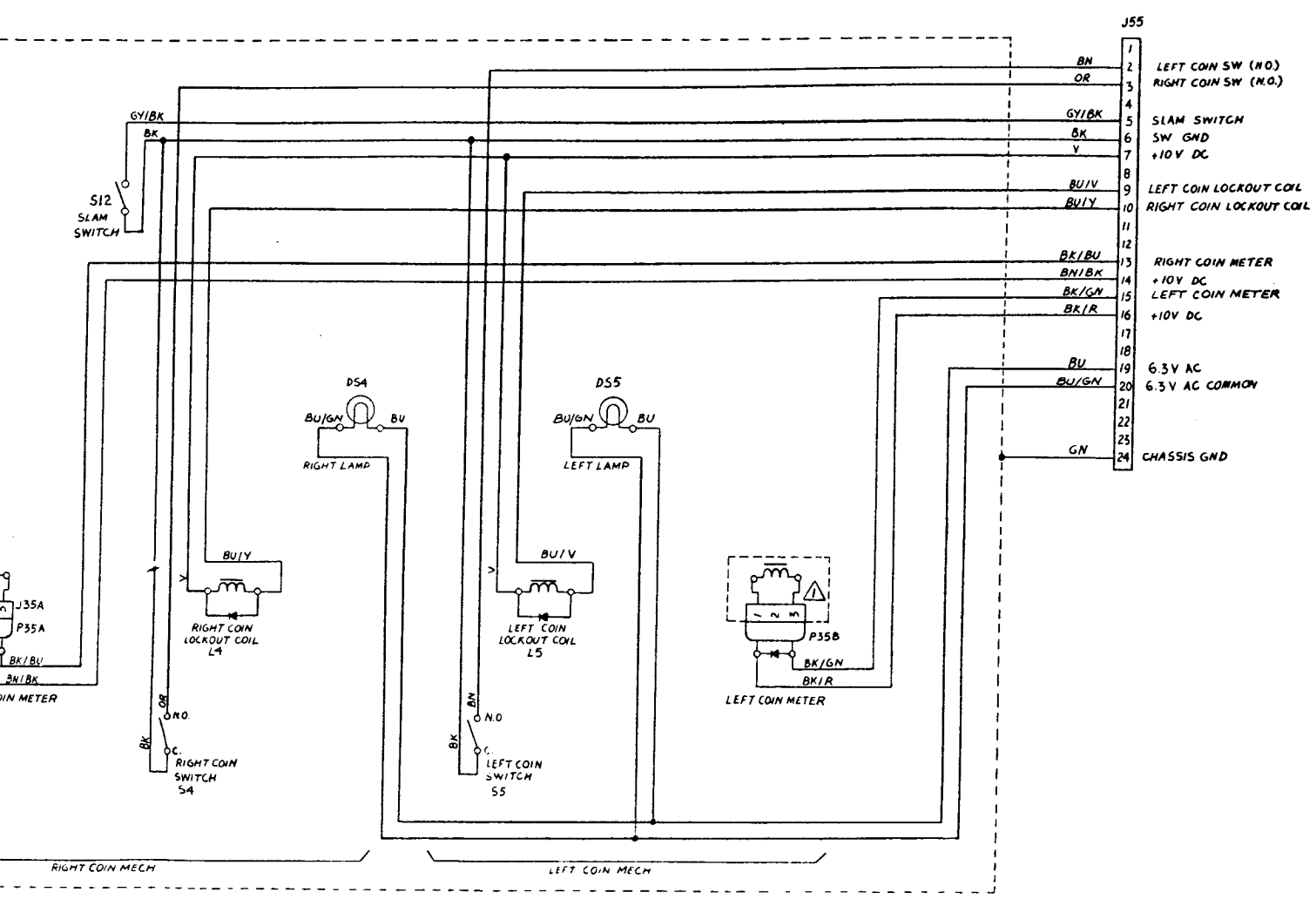


British-Made Coin D

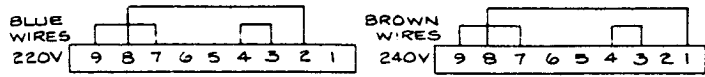




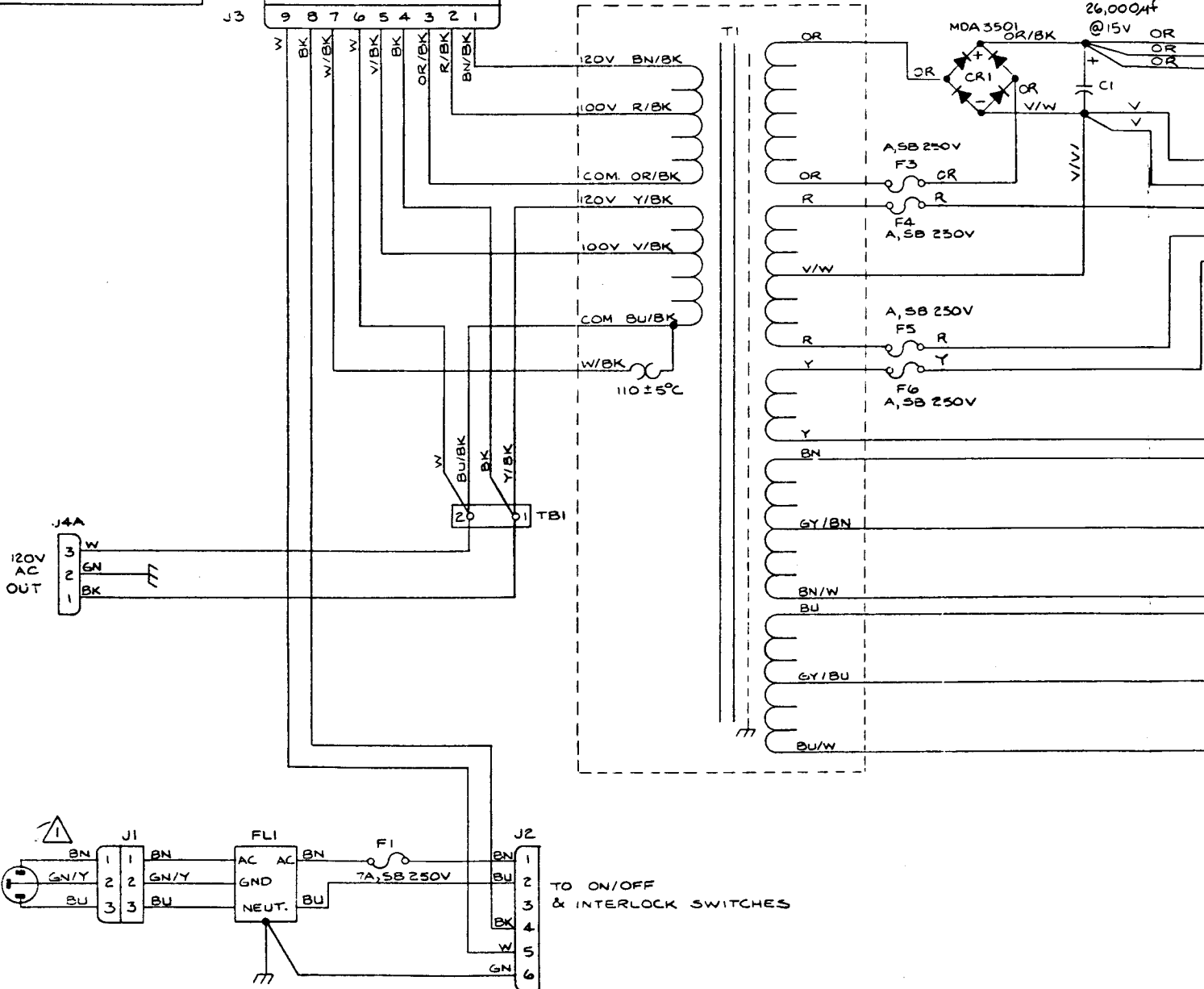
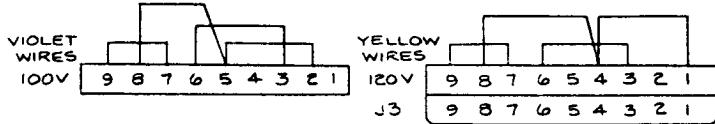
Coin Door Schematic (037050-01 A)

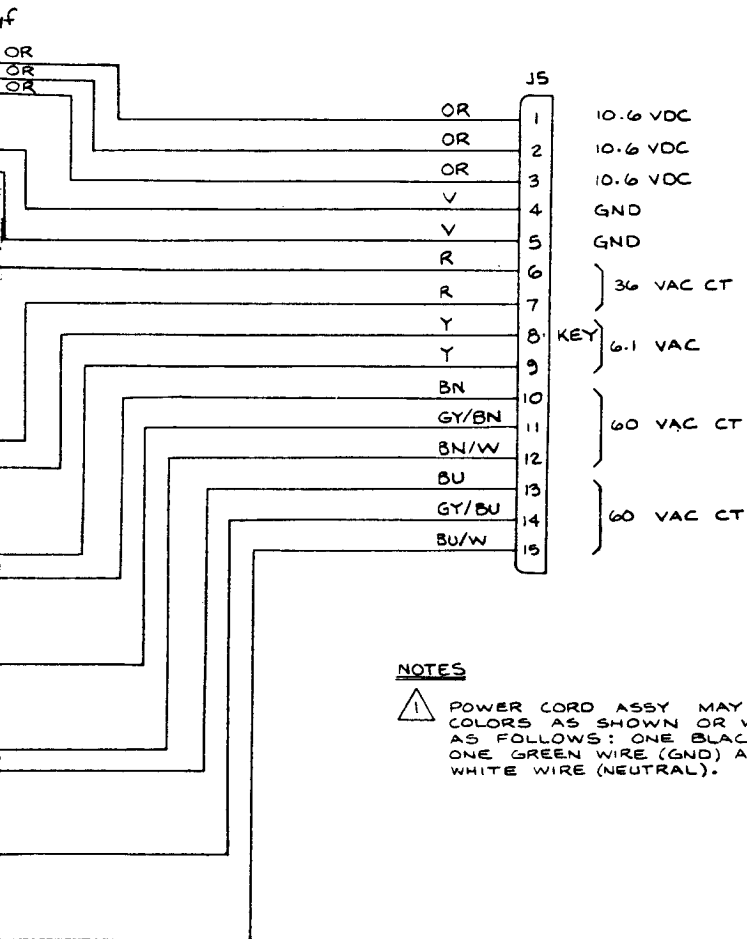


International Power Supply Schematic (037669-01 A)



VOLTAGE SELECTION BLOCKS





NOTES



POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).

Regulator Audio

Regulator/Audio II PCB

The Regulator/Audio II PCB has regulating the +5 VDC logic power to amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage pass transistor Q3 and Q3's driver transistor accurately regulates the logic power to the PCB by monitoring the voltage through the + SENSE and - SENSE. The regulator puts +5 VDC and ground inputs to the regulator regulates the voltage and eliminates a reduced voltage due to the harness between the regulator and resistor R8 is adjusted for the +5 VDC. Once adjusted, the voltage at the input remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 VDC and GND of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio II PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between the Regulator/Audio II PCB. Voltage should be greater than +5.5 VDC. If ground is not connected on both the game PCB and Regulator/Audio II PCB.
4. If cleaning PCB edge connectors, connect minus lead of voltmeter to GND test point of game PCB. Now connect minus lead of voltmeter to GND test point on Regulator/Audio II PCB. From the harness circuit is dropping the voltage to the appropriate harness wire color.

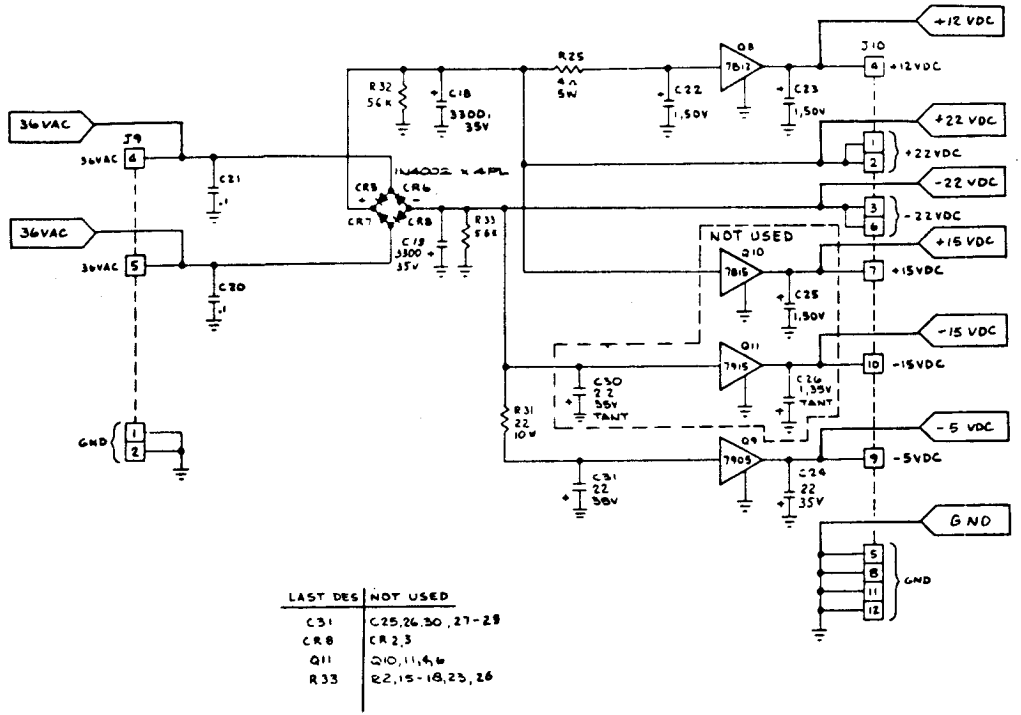
Audio Circuit

The audio circuit contains two amplifiers. Each amplifier consists of a transformer with an effective gain of 2.2.

PCB Schematic (035435-02 D)

dual functions of reg-
e game PCB and am-

regulator Q1, power
sistor Q2. The regula-
er input to the game
h high-impedance in-
puts are directly from
game PCB. Therefore,
the game PCB. This
IR loss in the wire
e game PCB. Variable
DC on the game PCB.
of the game PCB will



/ and GND test points

Regulator/Audio II
voltmeter.

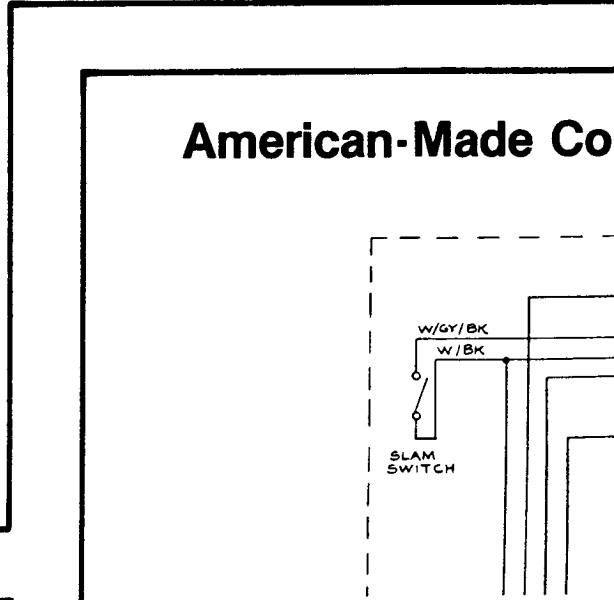
V REG and GND on
age reading must not
ter, try cleaning edge
PCB and the Regula-

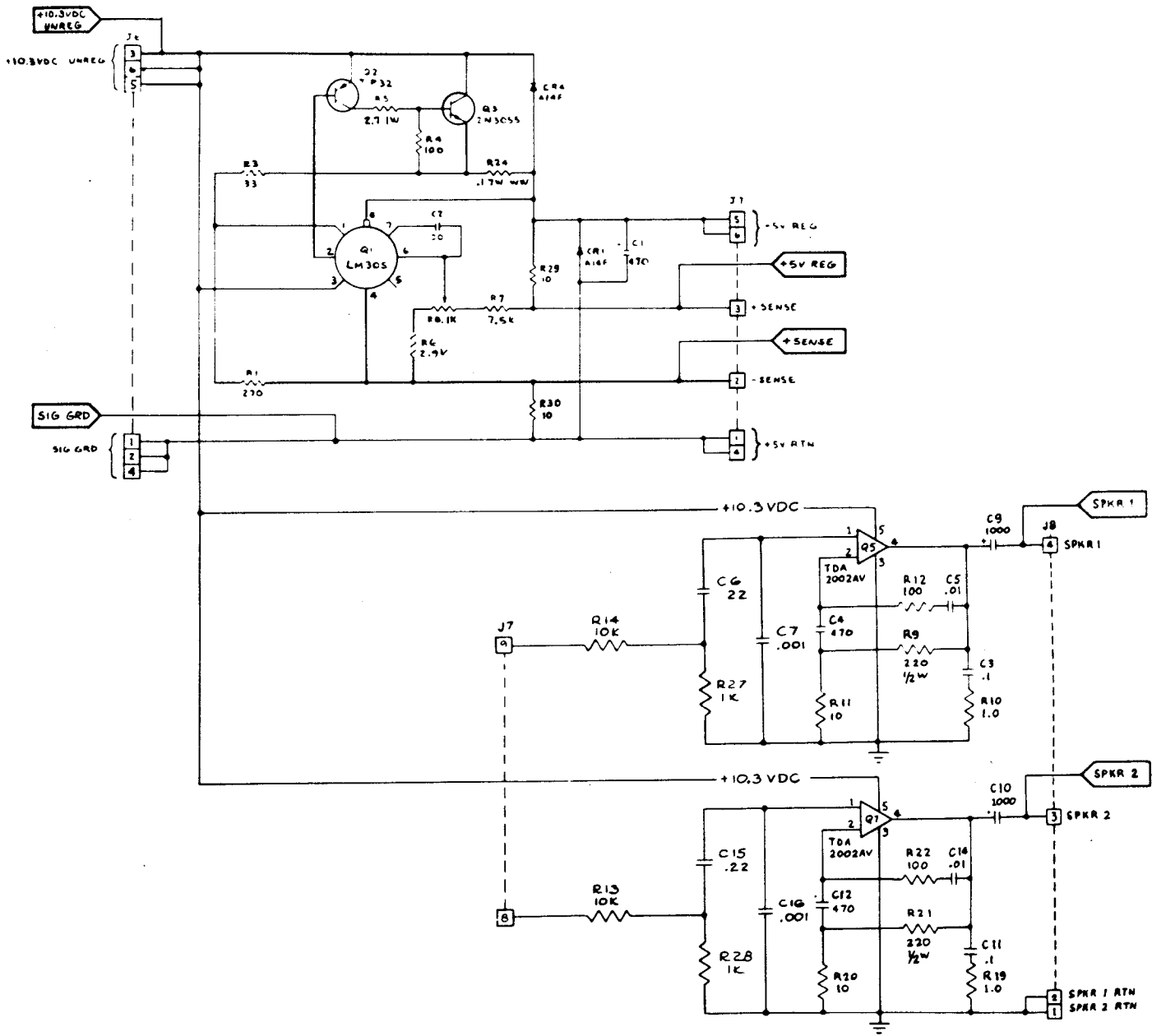
doesn't decrease volt-
d of voltmeter to GND
PCB and plus lead to
te the voltage.

meter to +5 REG test
nd plus lead to +5 V
is you can see which
oltage. Troubleshoot
arness connector.

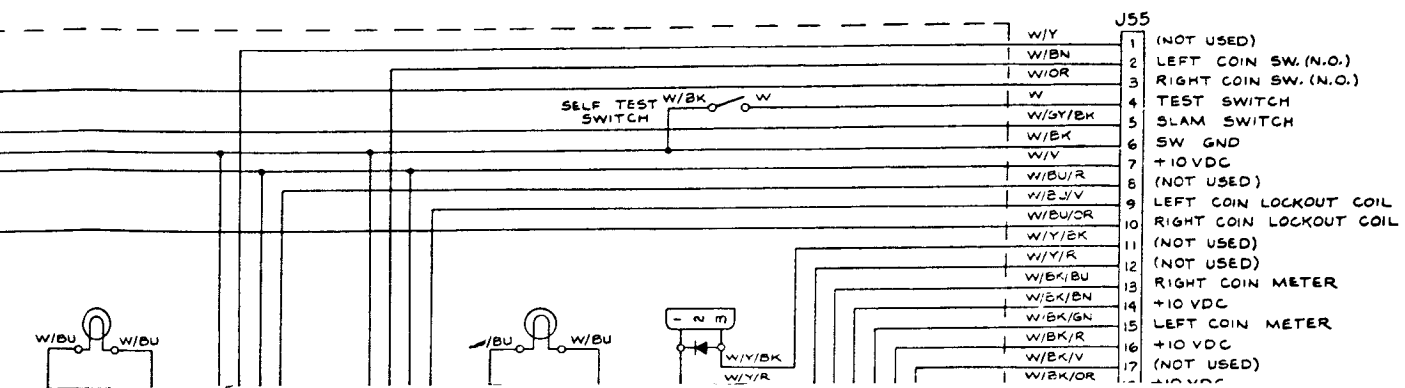
pendent audio ampli-
2002AV amplifier with

es a test point





Coin Door Schematic (036835-01 A)



Diagnostic Tests

Instruction	Use of Test																
<p>1. Hold the slam switch closed, while setting the self-test switch to the on position.</p>	<p>The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!</p> <table style="width: 100%; border: none;"> <tr> <td>Pale Yellow-Green</td> <td>Orange</td> <td>White</td> <td>Deep Yellow</td> </tr> <tr> <td>Light Green</td> <td>Dark Green</td> <td>Light Blue</td> <td>Lime Green</td> </tr> <tr> <td>Deep Rose</td> <td>Red</td> <td>Purple</td> <td>Red</td> </tr> <tr> <td>Navy Blue</td> <td>Black</td> <td>Royal Blue</td> <td>Black</td> </tr> </table>	Pale Yellow-Green	Orange	White	Deep Yellow	Light Green	Dark Green	Light Blue	Lime Green	Deep Rose	Red	Purple	Red	Navy Blue	Black	Royal Blue	Black
Pale Yellow-Green	Orange	White	Deep Yellow														
Light Green	Dark Green	Light Blue	Lime Green														
Deep Rose	Red	Purple	Red														
Navy Blue	Black	Royal Blue	Black														
<p>2. Activate any of the coin switches on the coin door.</p>	<p>A convergence pattern appears with a grid of white dots on a black screen. Do not attempt any convergence adjustments unless you are a qualified color TV technician!</p>																
<p>3. Set self-test switch to the off position.</p>	<p>Check attract-mode display and readjust brightness if necessary.</p>																

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFIDENTIAL: Reproduction forbidden without the specific written permission of Atari, Inc., Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof confers or transfers any right in, or license to use, the subject matter of the drawing or any design or technical information shown thereon, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendors of Atari, Inc., and for manufacture under the corporation's written license, no right to reproduce this drawing is granted or the subject matter thereof unless by written agreement with or written permission from the corporation.

Sheet 1, Side B



Centipede™

Synchronizer
Signature Analysis Procedure
CAT Box™ Preliminary Set-Up
Power Input
Microprocessor
Address Decoder
RAM
ROM
Memory Map

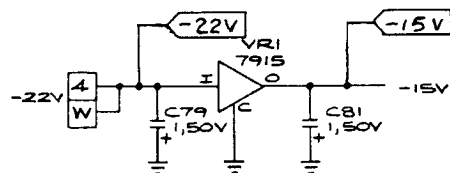
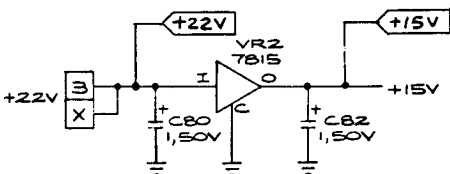
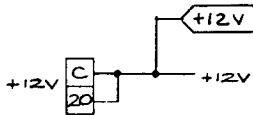
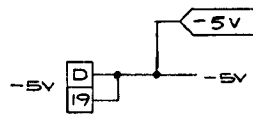
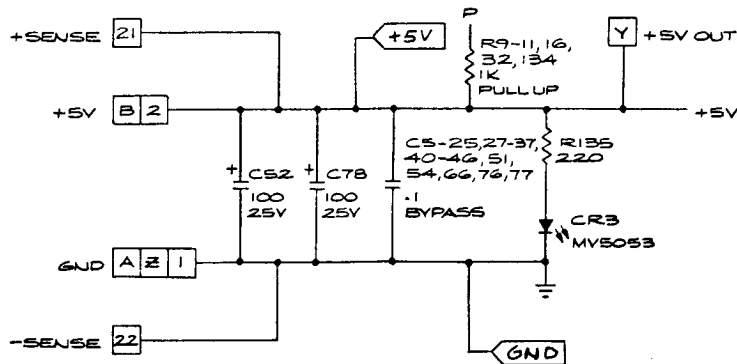
Section of 037241-01 B

© 1981 Atari, Inc.

A Warner Communications Company

◀ Denotes a test point

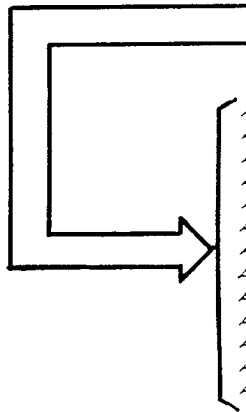
Power Input



◀ Denotes a test point

Testing the

1. Perform the CA
2. Set the CAT Bo
 - a. Press TEST
 - b. DBUS SOUR
 - c. BYTES to 10
 - d. R/W MODE
 - e. R/W to WRI
 - f. Key in 0000
 - g. Toggle R/W
 - h. R/W to REA
 - i. Toggle R/W
3. If the CAT Box r
PARE ERROR
shows the faili
PLAY switch is
4. If the COMPAR
peat the test w
ensures that th
COMPARE ERR
is good.



-02 VERSION
24K

◀ Denotes a test point

RAM

ox™ preliminary set-up.

switches as follows:

RESET
TO ADDR

OFF)

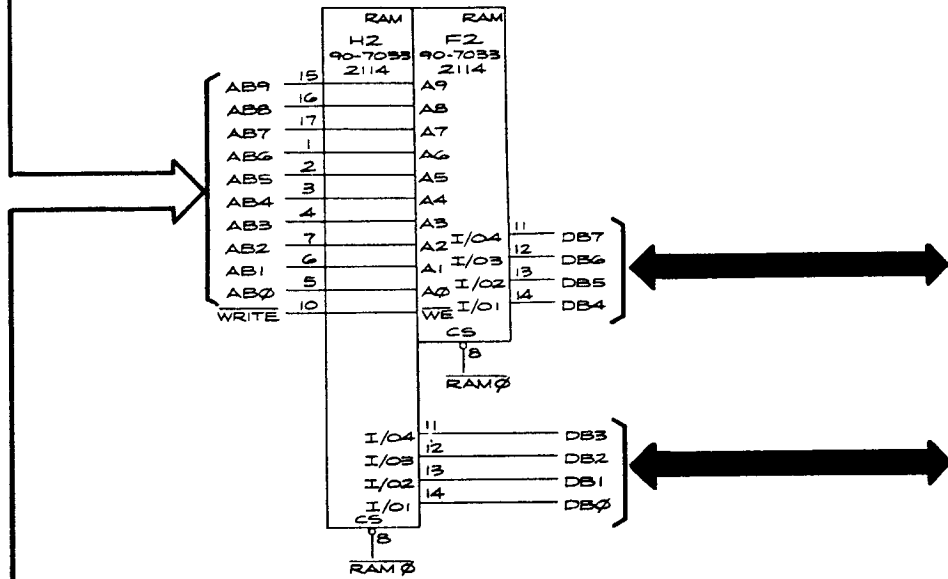
DE to SINGLE

DE to SINGLE

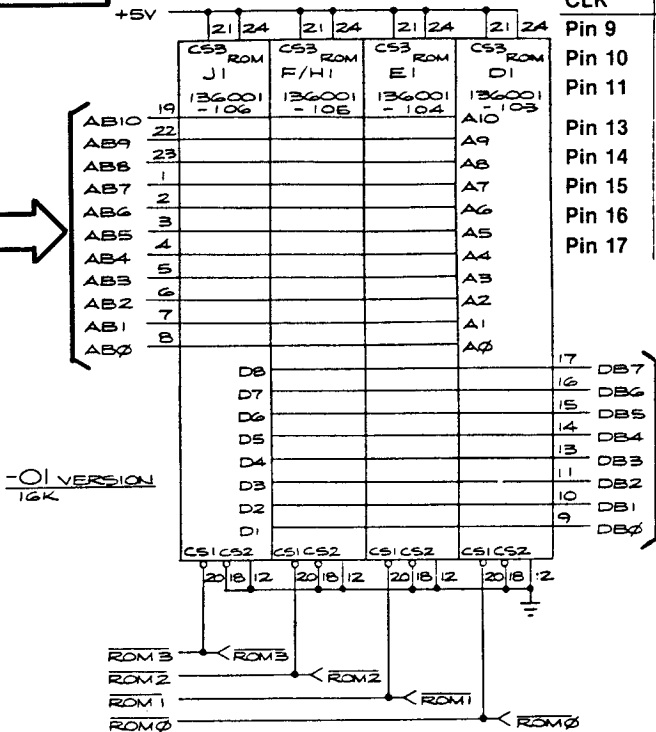
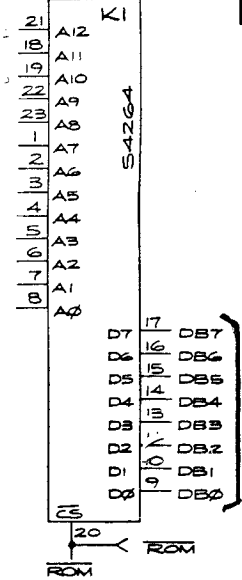
as an address that doesn't compare, the COM-
D) lights, the ADDRESS/SIGNATURE display
address location, and the ERROR DATA DIS-
abled.

ERROR LED does not light, rekey 0000 and re-
he DBUS SOURCE switch set to ADDR. This
ata bits at address 0000 will go high. If the
LED does not light after this step, the RAM

RAM



ROM



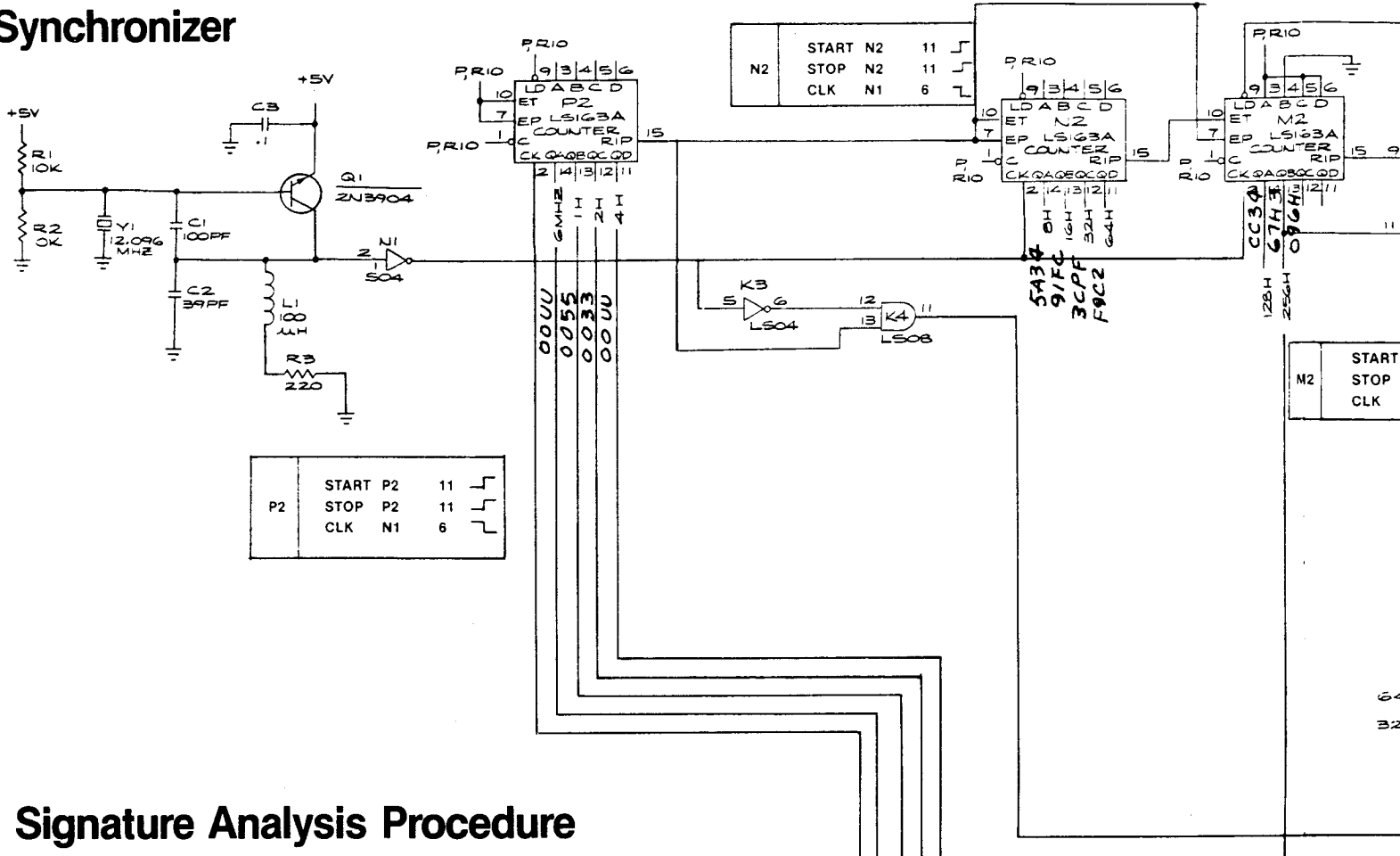
	D1	E1	F/H1	J1
START	Pin 20	Pin 20	Pin 20	Pin 20
STOP	Pin 20	Pin 20	Pin 20	Pin 20
CLK	φ2	φ2	φ2	φ2
Pin 9	OH81	13PH	CU62	476H
Pin 10	O8FC	C4P5	9553	2A2C
Pin 11	U9F7	11F3	7756	2337
Pin 13	P316	098P	A7CF	FP07
Pin 14	P8C4	5H24	6081	A9AF
Pin 15	H973	0548	5HAC	12HA
Pin 16	8F8F	33P7	6U43	2367
Pin 17	U638	80AA	F83H	8P82

Memory Map

MEMORY MAP										
HEXA-DECIMAL ADDRESS	R/W	DATA								FUNCTION
		D7	D6	D5	D4	D3	D2	D1	D0	
0000-03FF		D	D	D	D	D	D	D	D	RAM
0400-07BF 07C0-07CF 07D0-07DF 07E0-07EF 07F0-07FF		D	D	D	D	D	D	D	D	Playfield RAM Motion Object Picture Motion Object Vert. Motion Object Horiz. Motion Object Color
0800 0801	R R	D	D	D	D	D	D	D	D	Option Switch 1 (0 = On) Option Switch 2 (0 = On)
0C00 0C01 0C02 0C03	R R R R R R R R R R R	D					D	D	D	Horizontal Trak Ball™ Inputs VBLANK (1 = VBlank) Self-Test (0 = On) Cocktail Cabinet (1 = Cocktail) R,C,L Coin Switches (0 = On) SLAM (0 = On) Player 2 Fire Switch (0 = On) Player 1 Fire Switch (0 = On) Player 2 Start Switch (0 = On) Player 1 Start Switch (0 = On)
1000-100F 1404 140C 1600 1680 1700	R/W W W W W R	D	D	D	D	D	D	D	D	Custom Audio Chip Playfield Color RAM Motion Object Color RAM EA ROM Address & Data Latch EA ROM Control Latch EA ROM Read Data
1800	W									IRQ Acknowledge
1C00 1C01 1C02 1C03 1C04 1C07	W W W W W W	D								Left Coin Counter (1 = On) Center Coin Counter (1 = On) Right Coin Counter (1 = On) Player 1 Start LED (0 = On) Player 2 Start LED (0 = On) Trak Ball™ Flip Control (0 = Player 1)
2000 2400	W W									WATCHDOG Clear Trak Ball™ Counters
2000-3FFF	R									Program ROM

J1
Pin 20
Pin 20
φ2
476H
2A2C
2337
FP07
A9AF
12HA
2367
8P82

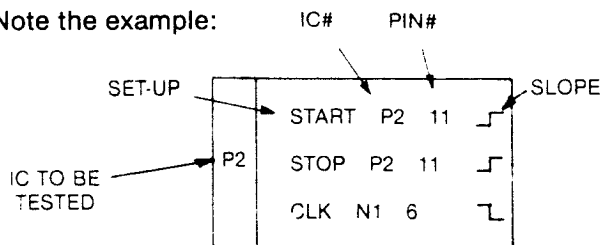
Synchronizer



Signature Analysis Procedure

1. Perform the CAT Box™ preliminary set-up.
2. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP, AND CLOCK jacks on the CAT Box.
3. Attach the three black E-Z clips to a ground loop on the CENTIPEDE™ game PCB.
4. Attach the CAT Box data probe to the DATA jack on the CAT Box.
5. The red E-Z clips on the cables will be moved about for each group of signatures to be taken. The set-up for each group of signatures is located on the schematic sheet near the device to be checked. The signatures are located on or near the signal point on the schematic.

Note the example:

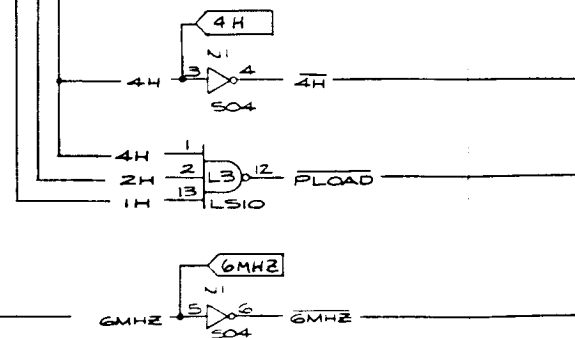


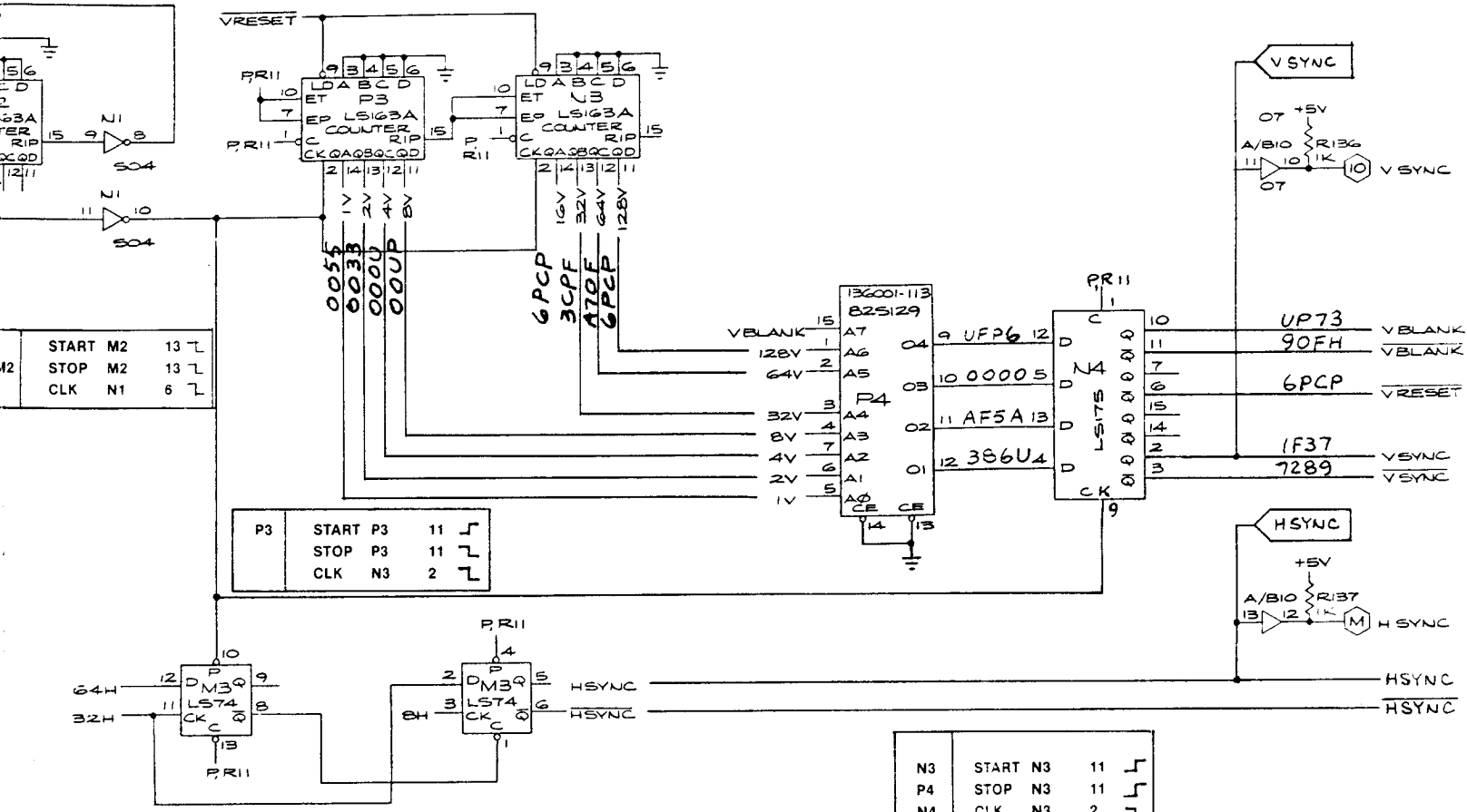
6. Set the CAT Box switches as follows:

- a. TESTER MODE: SIG
- b. TESTER SELF TEST: OFF
- c. PULSE MODE: LATCHED
- d. START:
- e. STOP:
- f. CLOCK:

CAT Box™ Preliminary

1. Remove:
 - The electrical power from the CAT Box.
 - The wiring harness from the CAT Box.
 - The game PCB from the CAT Box.
 - The MPU chip C2 from the CAT Box.
2. Connect:
 - The extender cables to the CAT Box.
 - Pins 37 to 39 on the MPU chip to the CAT Box.
 - The CAT Box flex cable to the CAT Box.

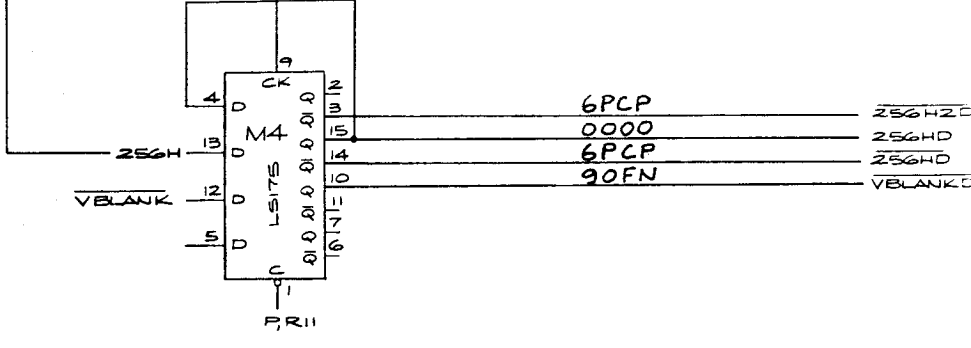




Preliminary Set-up

Power from the game.
 Address from the game PCB.
 Data from the cabinet.
 Clock from the game PCB.

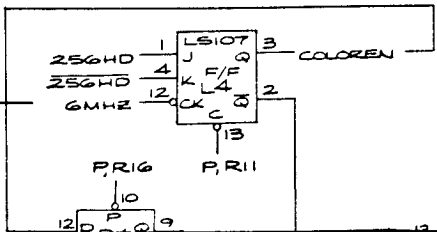
Connect the pins to the game PCB and the wiring harness.
 Connect the MPU socket with a piece of 28 AWG wire.
 Connect the cable to the game PCB test edge connector.



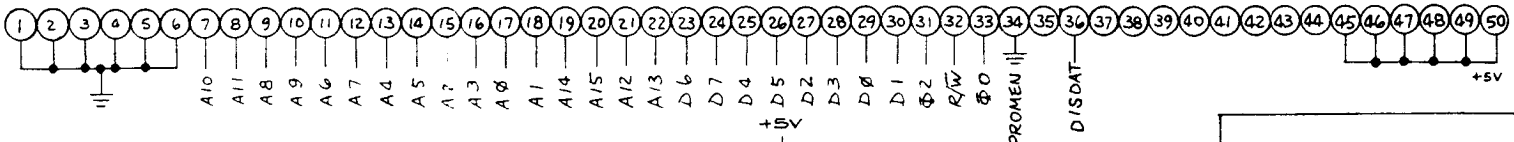
4H

LOAD

6MHz

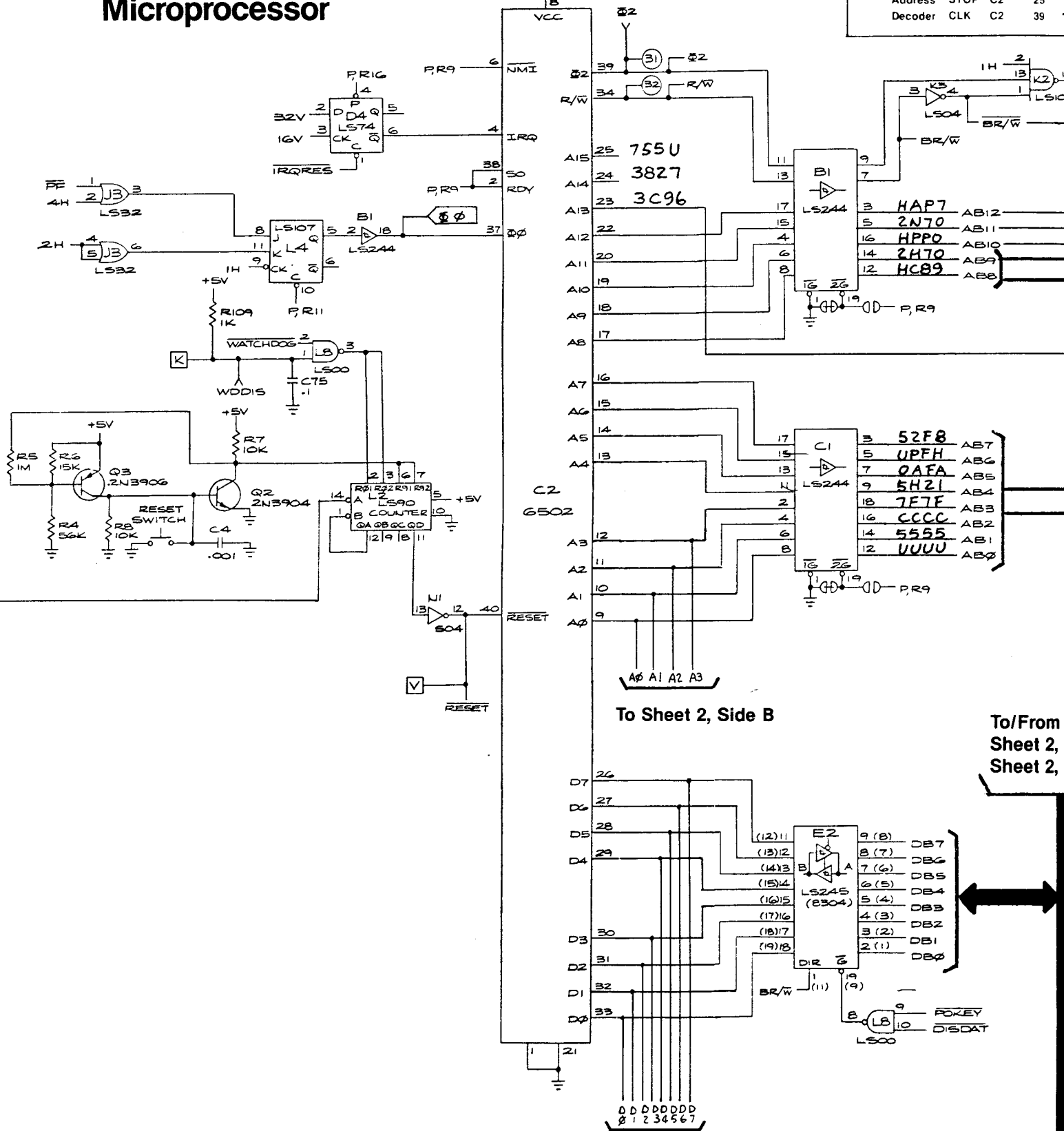


TEST CONNECTOR-FOR ATARI CAT BOX™



Microprocessor

MPU & Address Decoder	START C2	25	7
	STOP C2	25	7
	CLK C2	39	7



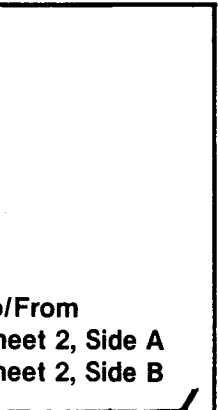
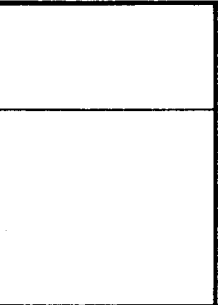
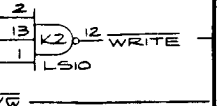
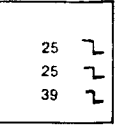
To Sheet 2, Side B

To/From Sheet 2, S Sheet 2, S

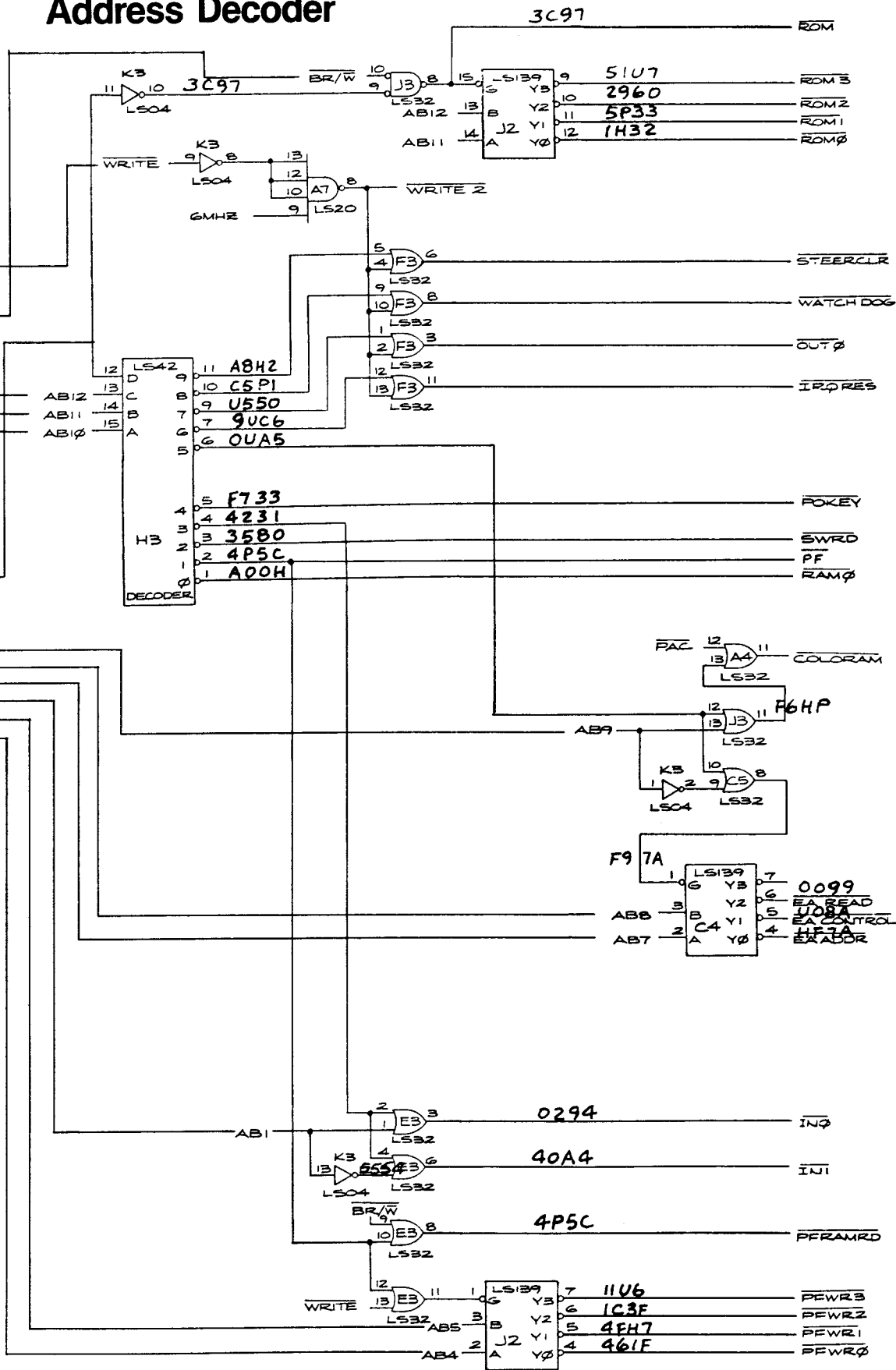
To/From Sheet 2, Side B

Address Decoder

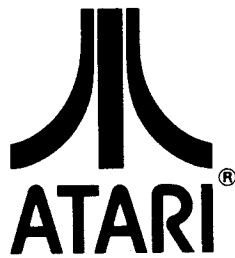
To/From
Sheet 2, Side A
Sheet 2, Side B



To/From
Sheet 2, Side A
Sheet 2, Side B



NOTE:
To obtain proper signature



Sheet 2, Side A

Centipede™

**Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry (Vertical)
Motion Object Circuitry (Horizontal)
Section of 037241-01 C +**

© 1981 Atari, Inc.



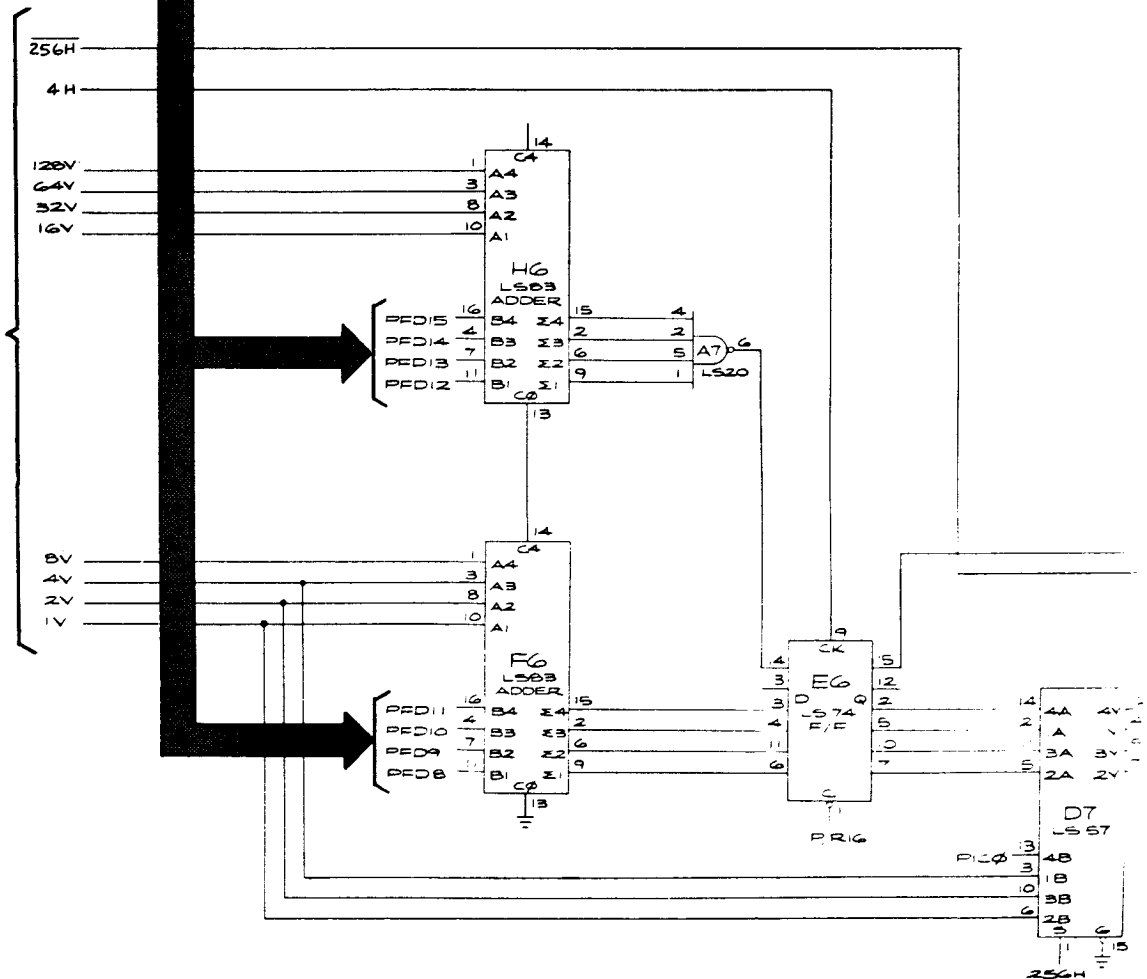
A Warner Communications Company

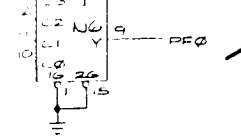
Motion Object Circuitry (Vertical)

The Motion Object Circuitry (vertical) receives playfield data and sync generator circuitry to generate the vertical component of the motion object. The 15 from the playfield memory and 1V-128V from the sync generator are selected by A7. The output is gated by A7 when a motion object is on one of the six vertical lines. A low on B7 pin 8 indicates the presence of a motion object on one of the vertical lines during non-active video time. This signal (MGA) is used by the picture data multiplexers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PIC0 are selected. The latched output of E6 is selected. The output of D7 is EXCLUSIVE OR gate E7. The output of E7 is sent to the picture data selector circuitry as motion graphic address. The input to EXCLUSIVE OR gate E7 is PIC7 from the playfield code memory. When high causes the output of E7 to be complimented. For example, PIC7 causes MGA0-MGA3 to go high. This causes the motion object to go to bottom.

From Sync Generator Sheet 1, Side B



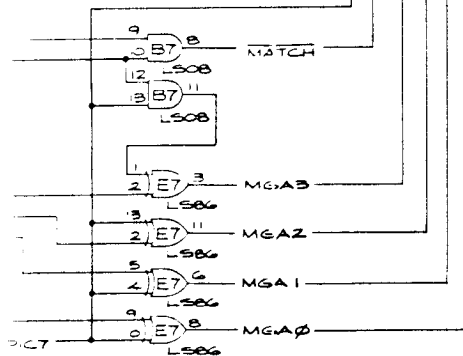
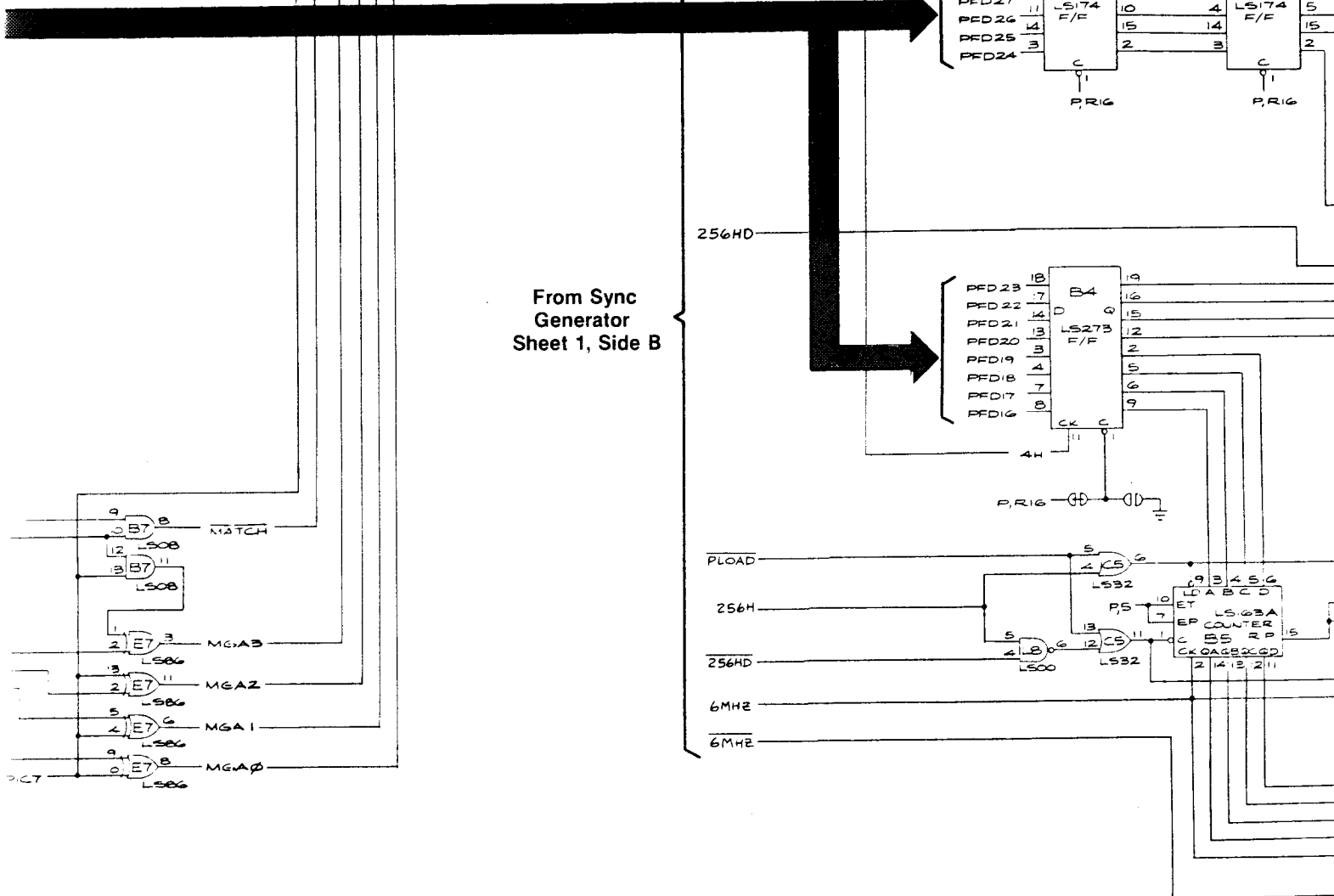


Motion Object Circuitry (Horizontal)

The motion object circuitry (horizontal) receives playfield data and horizontal sync data from the sync generator circuitry. PFD16-PFD23 from the playfield memory determine the position of the motion object. PFD24-PFD29 from the playfield memory determine the color of the motion object. PFD16-PFD23 are latched by L7 and loaded into the horizontal position counters A5 and B5 by a low on pin 9. The horizontal position counters then output data to RAMs A6 and B6. These RAMs are loaded with the video data for the particular motion object from shift registers H9 and J9 (which were loaded from the graphics ROM). The data from RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.

cal inputs from the motion object video. PFD8-PFD15 are compared at F6 and H6. The outputs of these comparators are used to determine vertical lines and is used to determine a motion object on the screen. This circuitry enables the multi-

When 256H goes low, the circuitry is gated at E7 and is inverted (GA0-MGA3). The other logic circuitry. PIC7 GA0-MGA3 are low, so to be inverted top

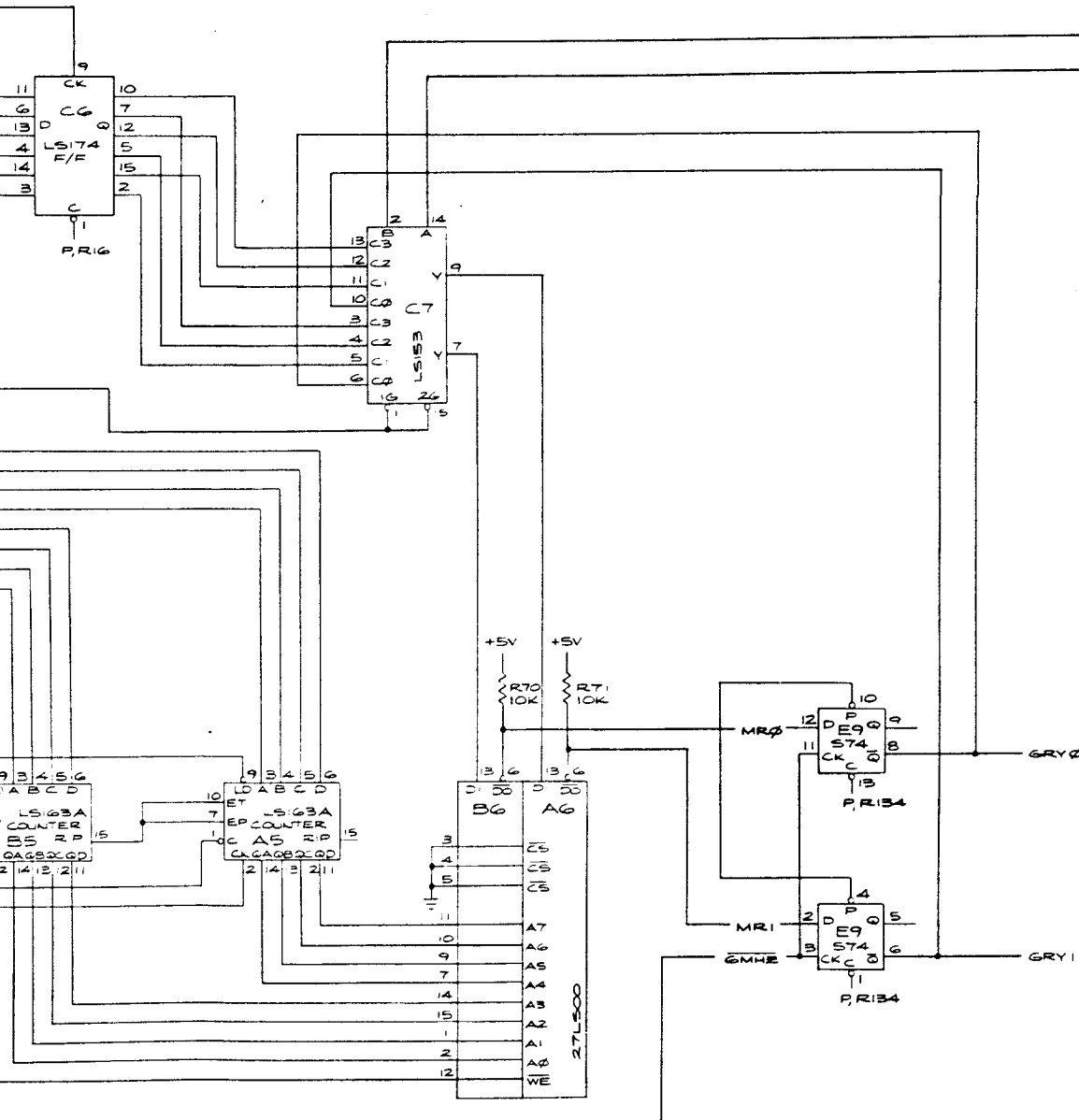


Horizontal)

...a and horizontal inputs from memory determine the horizontal memory determine the indirect address into the horizontal position counters then address video the particular motion object (graphics ROM). The output for R0 and MR1.

playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and 256H from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16 line by 8 bit blocks of motion object video.

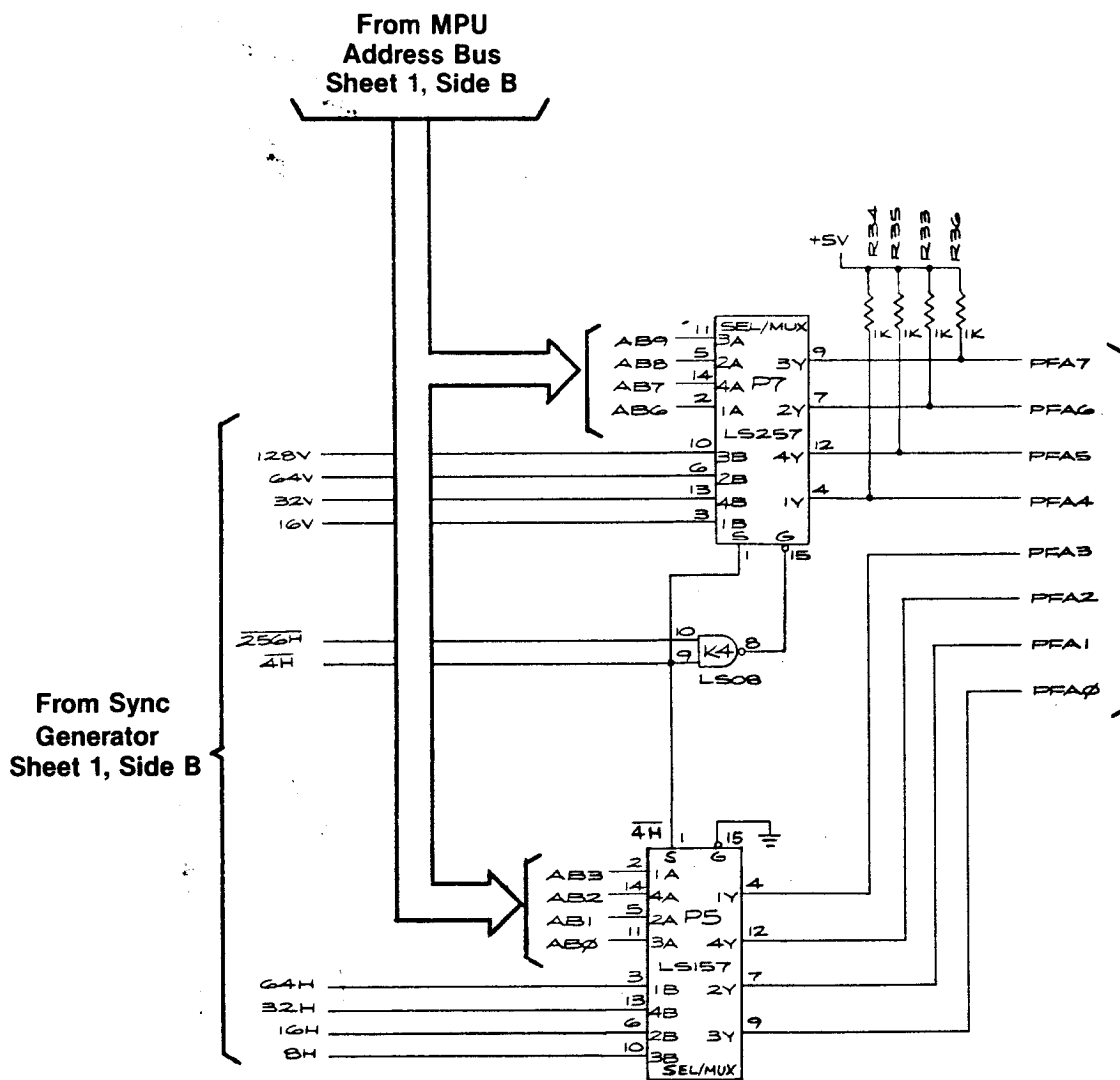
256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM output D1-D8 on F7 and H/J7 are multiplexed by F8, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.



Centipede PL

Testing the P

1. Perform the CAT E
2. Set the CAT Box s
 - a. Press TESTER I
 - b. DBUS SOURCE
 - c. BYTES to 1024
 - d. R/W MODE to (
 - e. R/W to WRITE
 - f. Key in 0400
 - g. Set R/W MODE
 - h. R/W to READ
 - i. Set R/W MODE



Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When $\overline{4H}$ on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When $\overline{4H}$ goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

Code Playfield RAM

the Playfield RAM

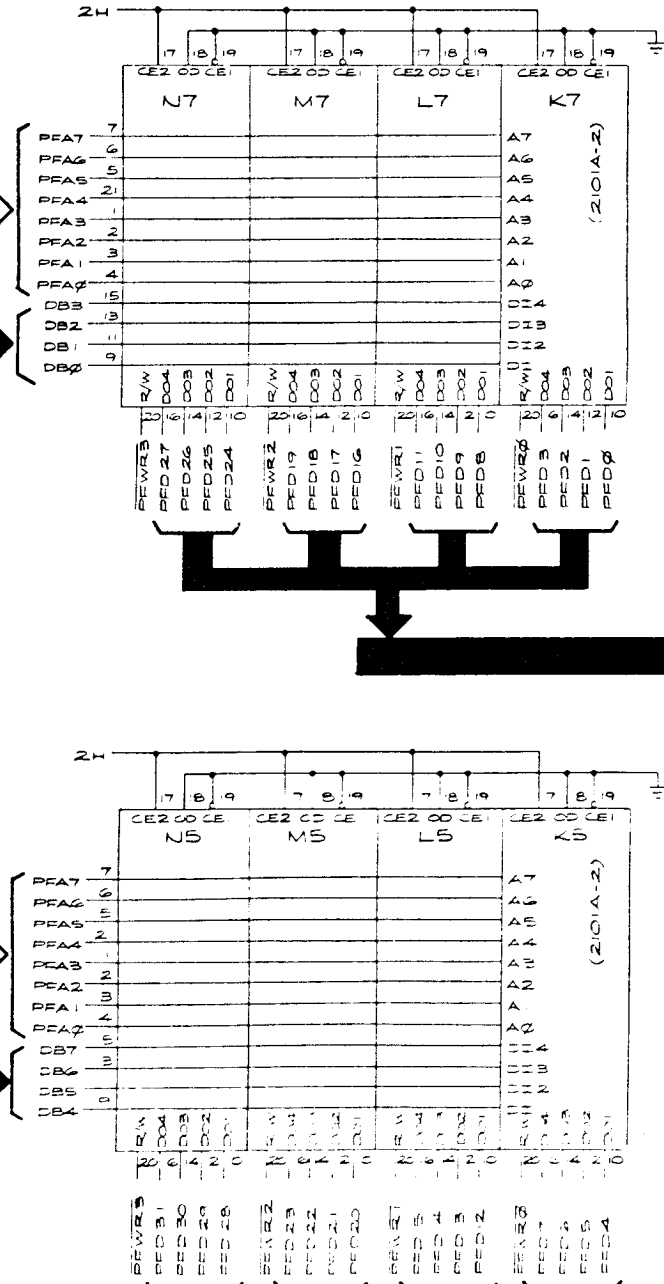
the CAT Box preliminary set-up.

CAT Box switches as follows:

- TESTER RESET
- SOURCE TO ADDR
- S to 1024
- MODE to (OFF)
- WRITE
- 0400
- W MODE to PULSE, then to OFF.
- READ
- W MODE to PULSE, then to OFF.

3. If the CAT Box reads an address that doesn't compare, the COMPARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled.
4. If the COMPARE ERROR LED does not light, rekey 0400 and repeat the test with the DBUS SOURCE switch set to ADDR. This ensures that the data bits at address 0400 will go high. If the COMPARE ERROR LED does not light after this step, the Playfield RAM is good.

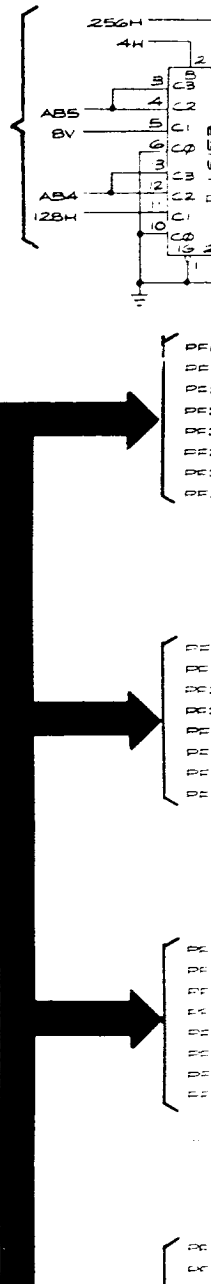
To/From MPU
Data Bus
Sheet 1, Side B



The PI
(PF0-PF
played on
consists

When 2
selected
as select
playfield
is low, th
These sig
M6, and

The pl
and to th
sync gen
DB0-DB7.
picture d

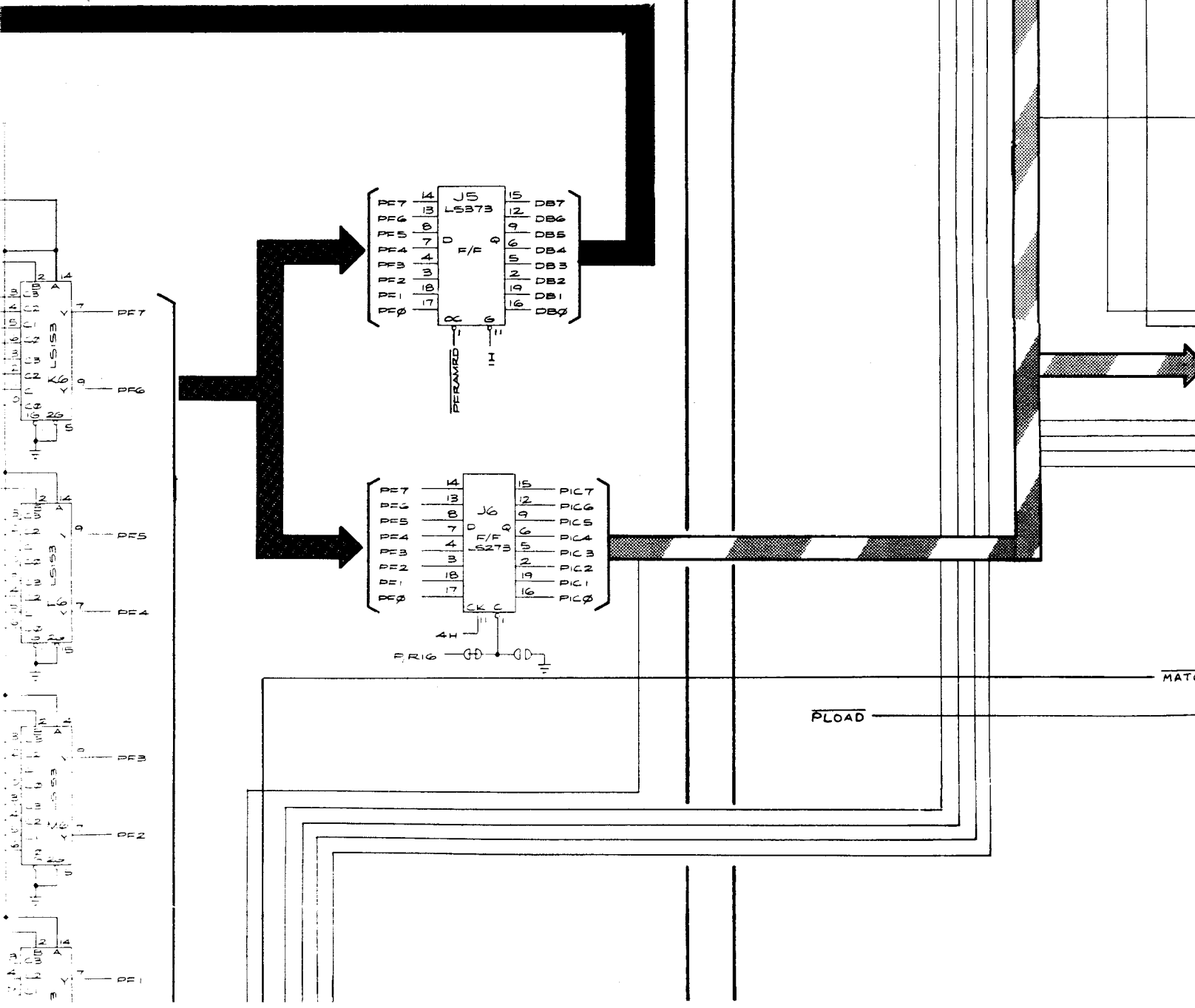


Playfield Multiplexer

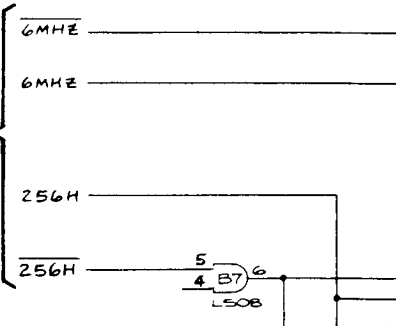
The Multiplexer receives playfield data from the playfield memory and the output (PF0-PF7) is a code that determines what is 1) displayed on the monitor, or 2) read or updated by the MPU. The Playfield Multiplexer consists of eight multiplexers K6, L6, M6, N6 and P6.

When 4H is low and 4H is high, AB4 and AB5 from the MPU address bus is the code from P6. This output is applied to multiplexers K6, L6, M6, and N6. When the MPU is accessing the playfield code multiplexer, the code is either being read or updated by the MPU. When 256H is high and 4H is low, the outputs from the sync generator (128H and 8V) are the selected outputs. When 256H is high and 4H is high, the outputs from the sync generator (128H and 8V) are the selected outputs. When 256H is high and 4H is high, the outputs from the sync generator (128H and 8V) are the selected outputs.

The playfield codes (PF0-PF7) are latched by J5 and J6 to the MPU data bus (J5) and to the data PROM circuitry (J6). When PFRAMD is low and 1H from the MPU address bus goes high, the inputs on J5 (PF0-PF7) are latched out to the MPU via J5. When 4H on pin 11 of J6 goes high, the inputs (PF0-PF7) are latched to the data PROM circuitry.

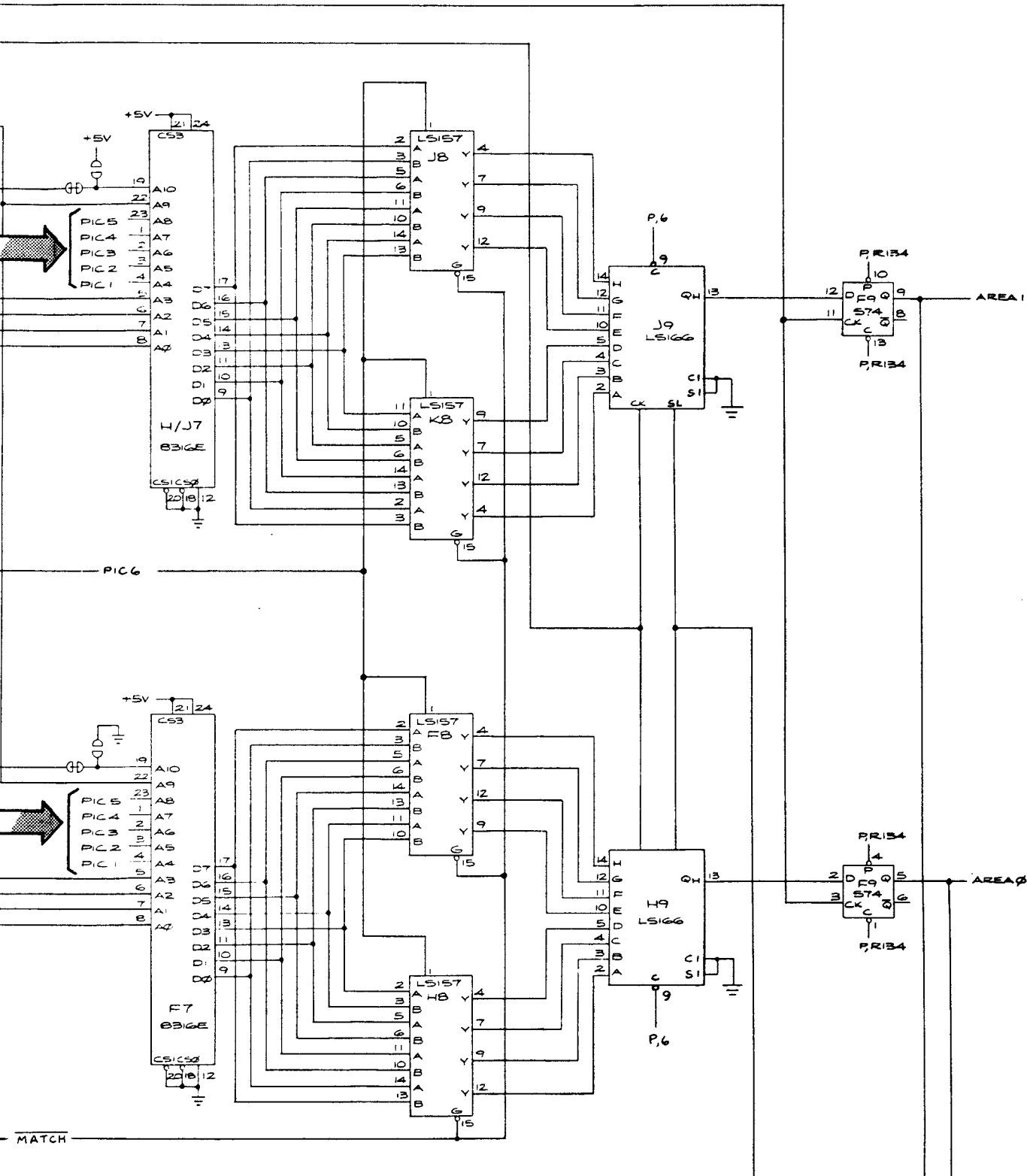


From Sync Generator Sheet 1, Side B



FLOOD

MAT



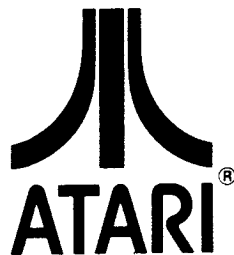
Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/J7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.

Testing the Option Switches

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
 - a. DBUS SOURCE to DATA
 - b. BYTES to 1
 - c. R/W to READ
 - d. Key in address 0800 (N9) or 0801 (N8)
 - e. R/W MODE to STATIC
3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
CONFIDENTIAL: Reproduction forbidden without the specific written permission of Atari, Inc., Sunnyvale, CA. This drawing is only conditionally issued, and neither receipt nor possession thereof confers or transfers any right in, or license to use, the subject matter of the drawing or any design or technical information shown thereon, nor any right to reproduce this drawing or any part thereof. Except for manufacture by vendor of Atari, Inc., and for manufacture under the corporation's written license, no right to reproduce this drawing is granted or the subject matter thereof unless by written agreement with or written permission from the corporation.



Sheet 2, Side B

Centipede™

Joystick Circuitry
Mini-Trak Ball™ Circuitry
Player Input Circuitry
Video Output Circuitry
Audio Output Circuitry
Coin Counter Output Circuitry
Option Input Circuitry
High Score Memory Circuitry

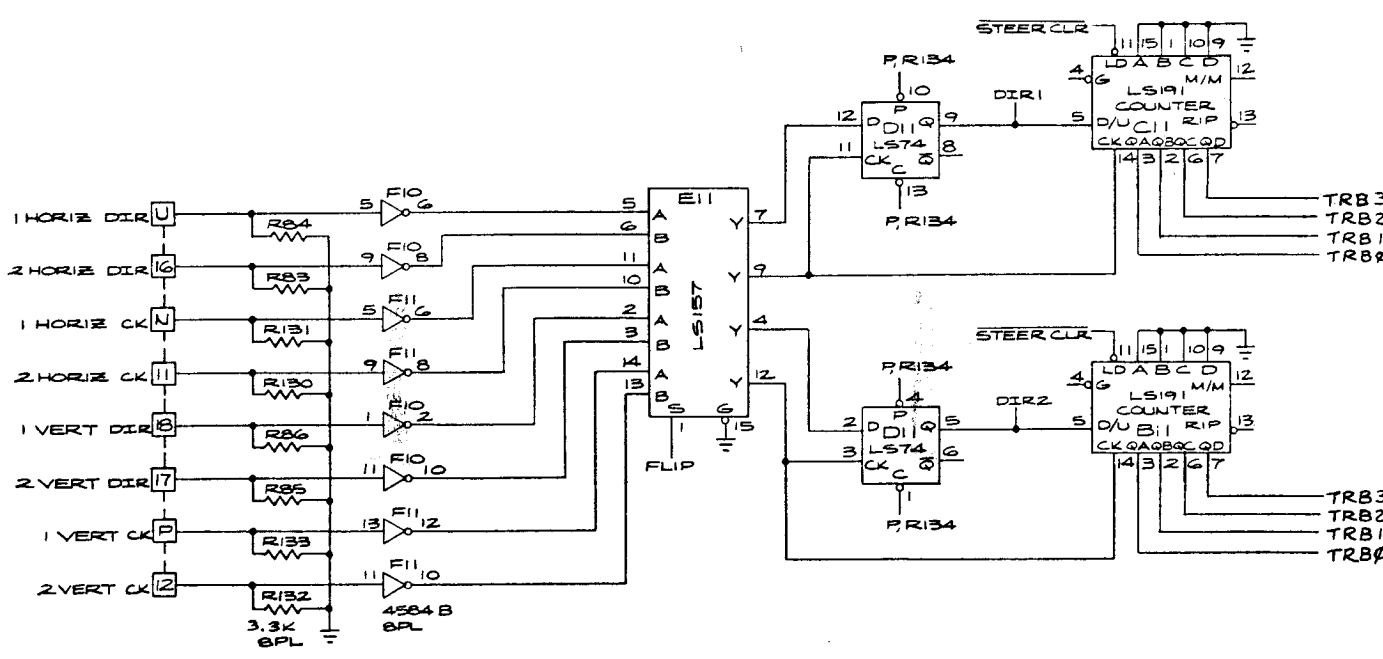
Section of 037241-01 C +

© 1981 Atari, Inc.

Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on AB0-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Mini-Trak Ball™ Circuitry



Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
 - a. DBUS SOURCE to DATA
 - b. BYTES to 1
 - c. R/W to READ
 - d. Key in address 0C00 (vertical) or 0C02 (horizontal)
 - e. R/W MODE to PULSE
3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.

vide 6 extra colors for a total of 14.

1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 3. The result is a pale blue when COLOR 1 and COLOR 2 are off.
2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 2. The result is a pale green when COLOR 1 and COLOR 3 are off.

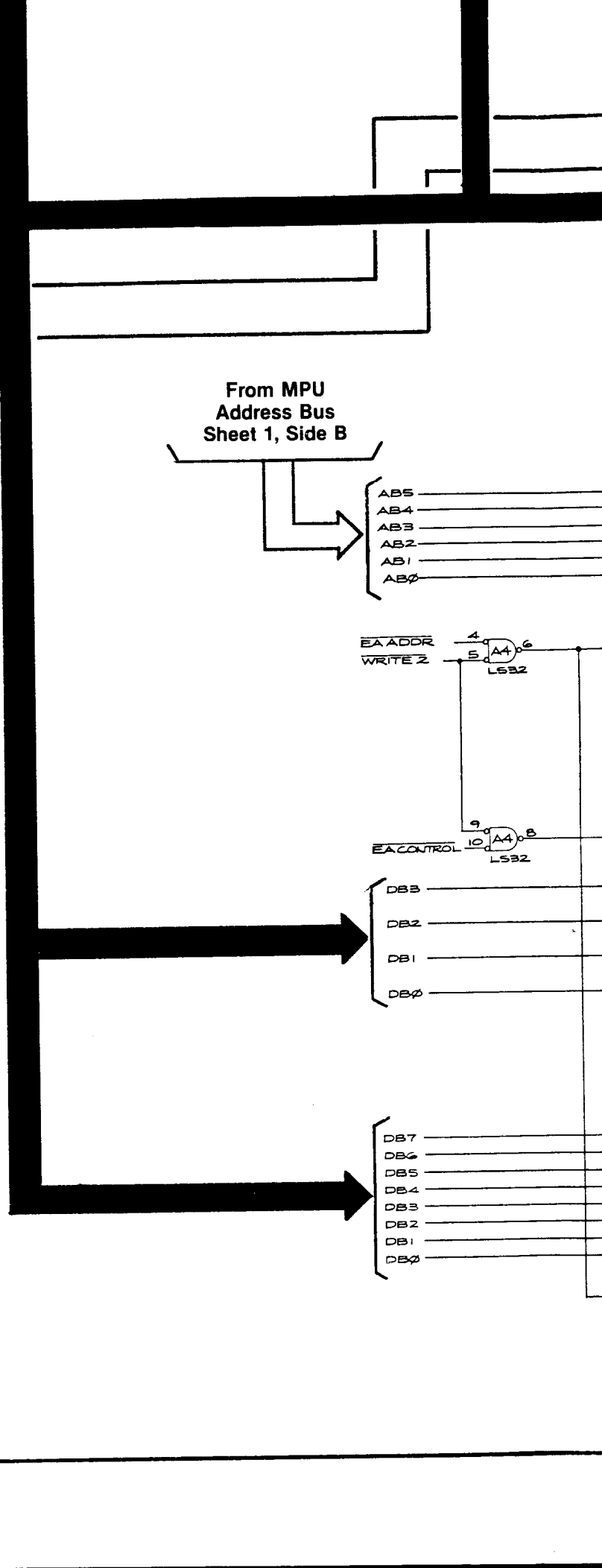
High Score Memory Circuitry

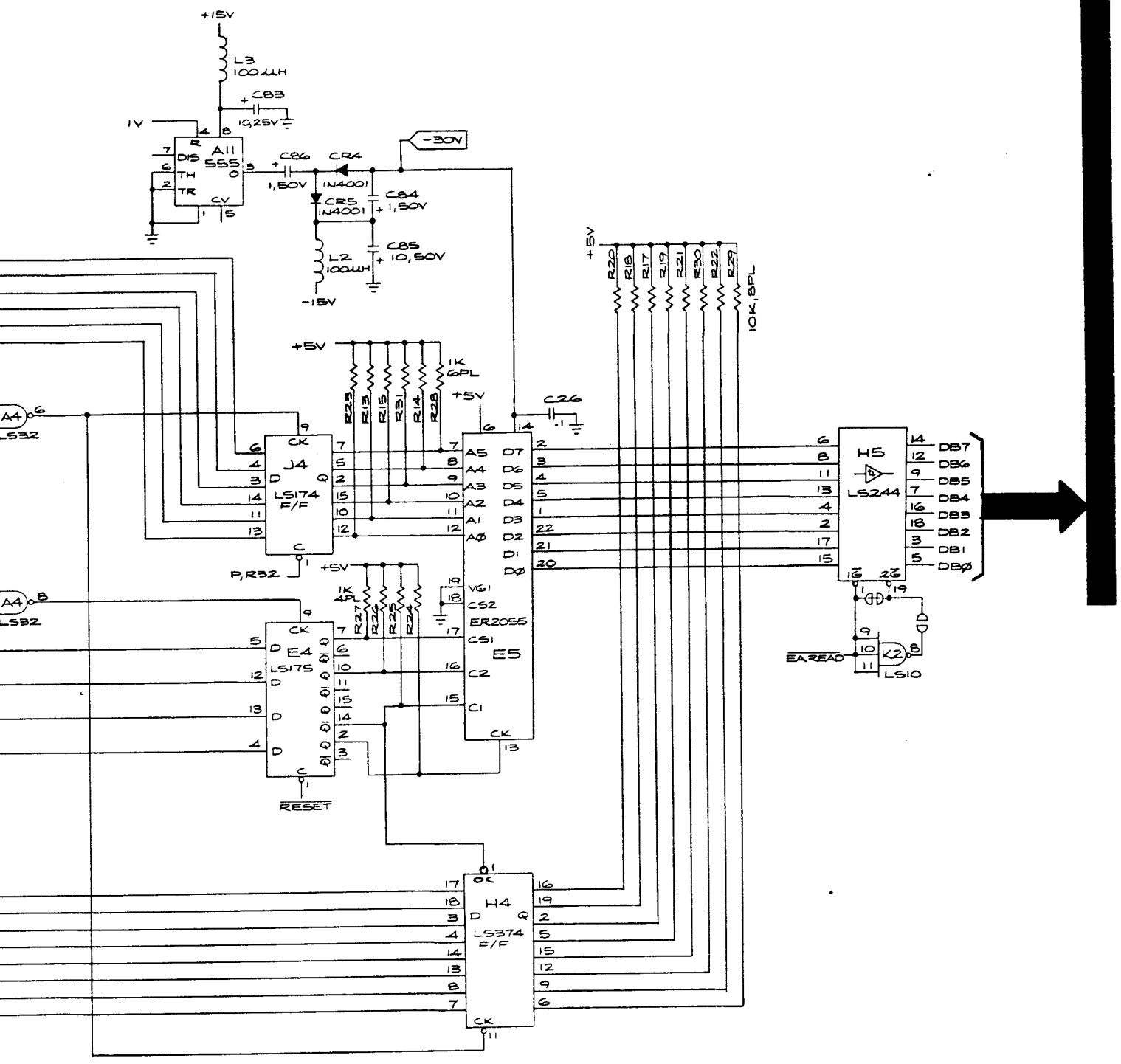
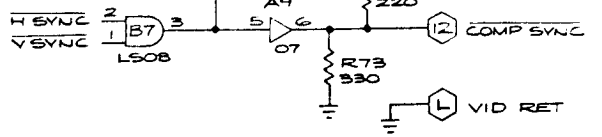
The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5 and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to -29V. When the signal is 0V, CR5 is cutoff and CR4 is forward-biased which causes C84 to develop a charge. C84 charges to approximately -28V. This is the potential required for EAROM C0 to operate.

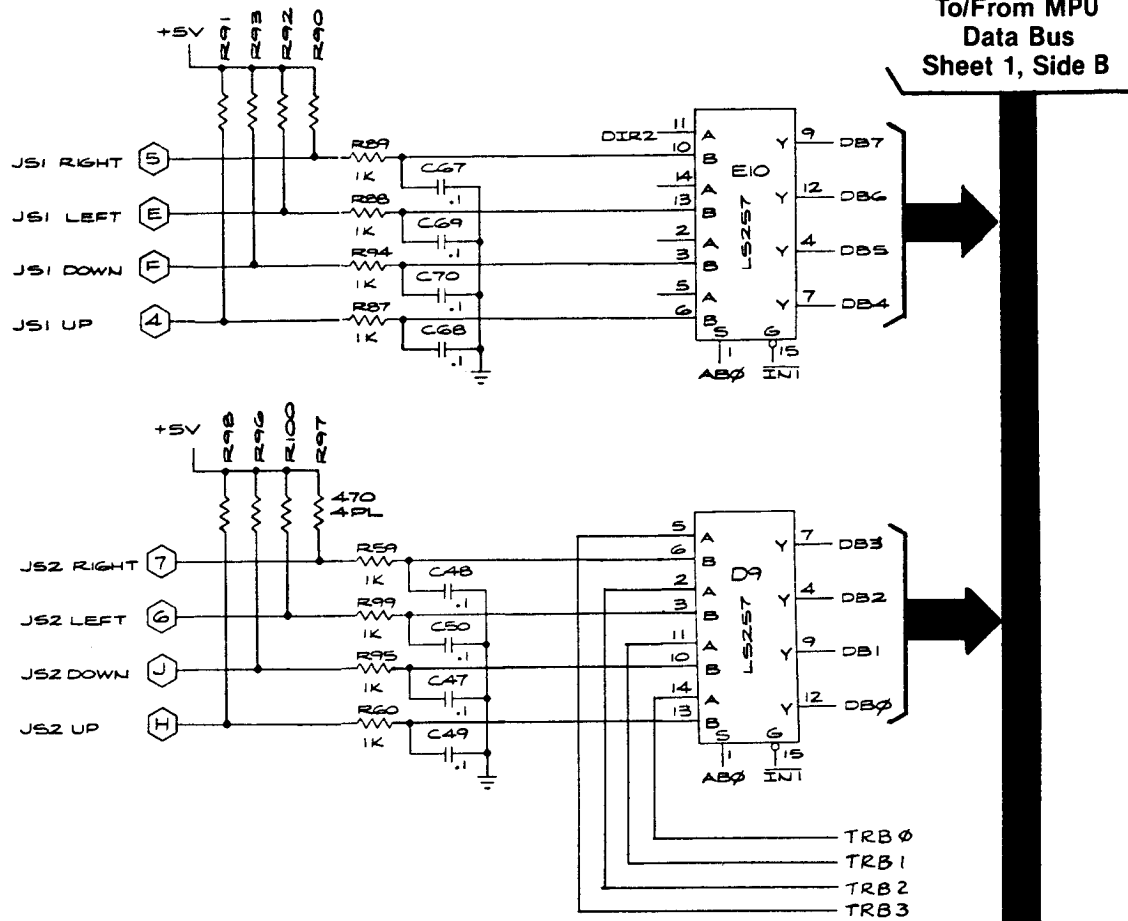
The MPU addresses the EAROM (AB0-AB5) when a low \overline{EAADDR} gates $\overline{WRITE2}$ at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low $\overline{EACONTROL}$ gates $\overline{WRITE2}$ at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when \overline{EAREAD} on pin 1 of buffer H4 goes low.

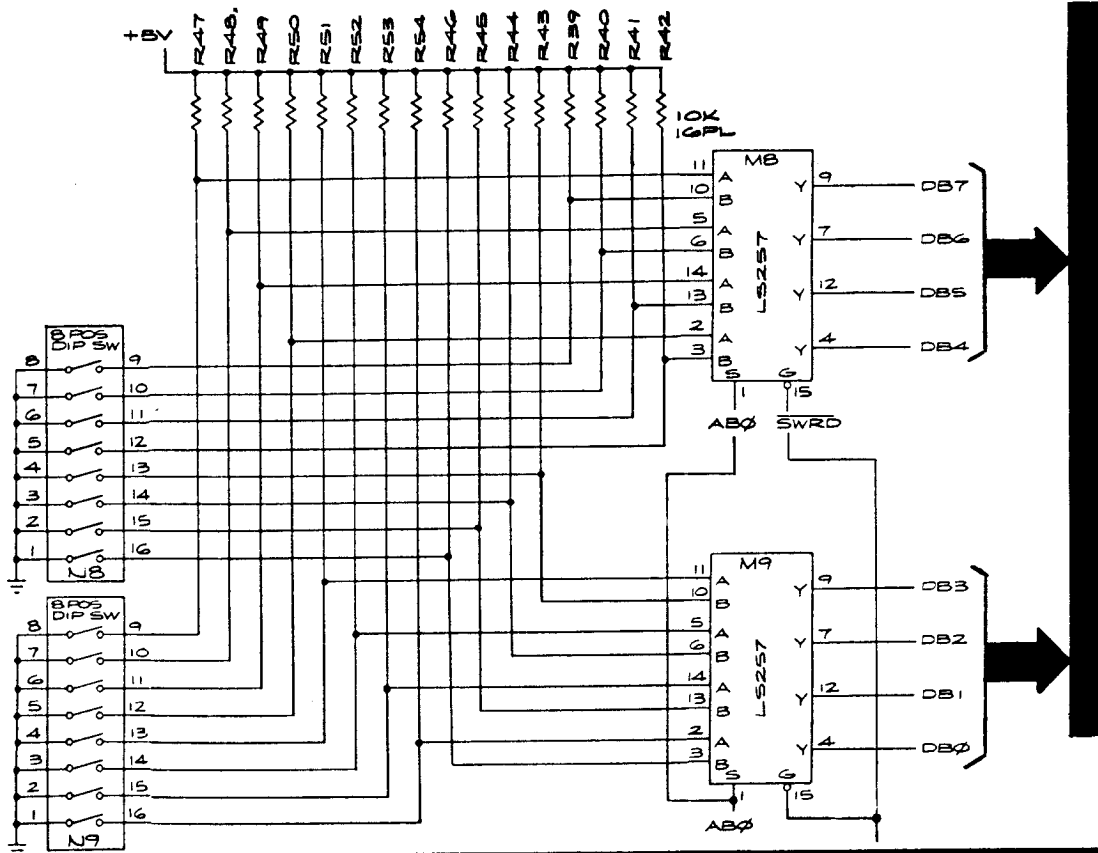




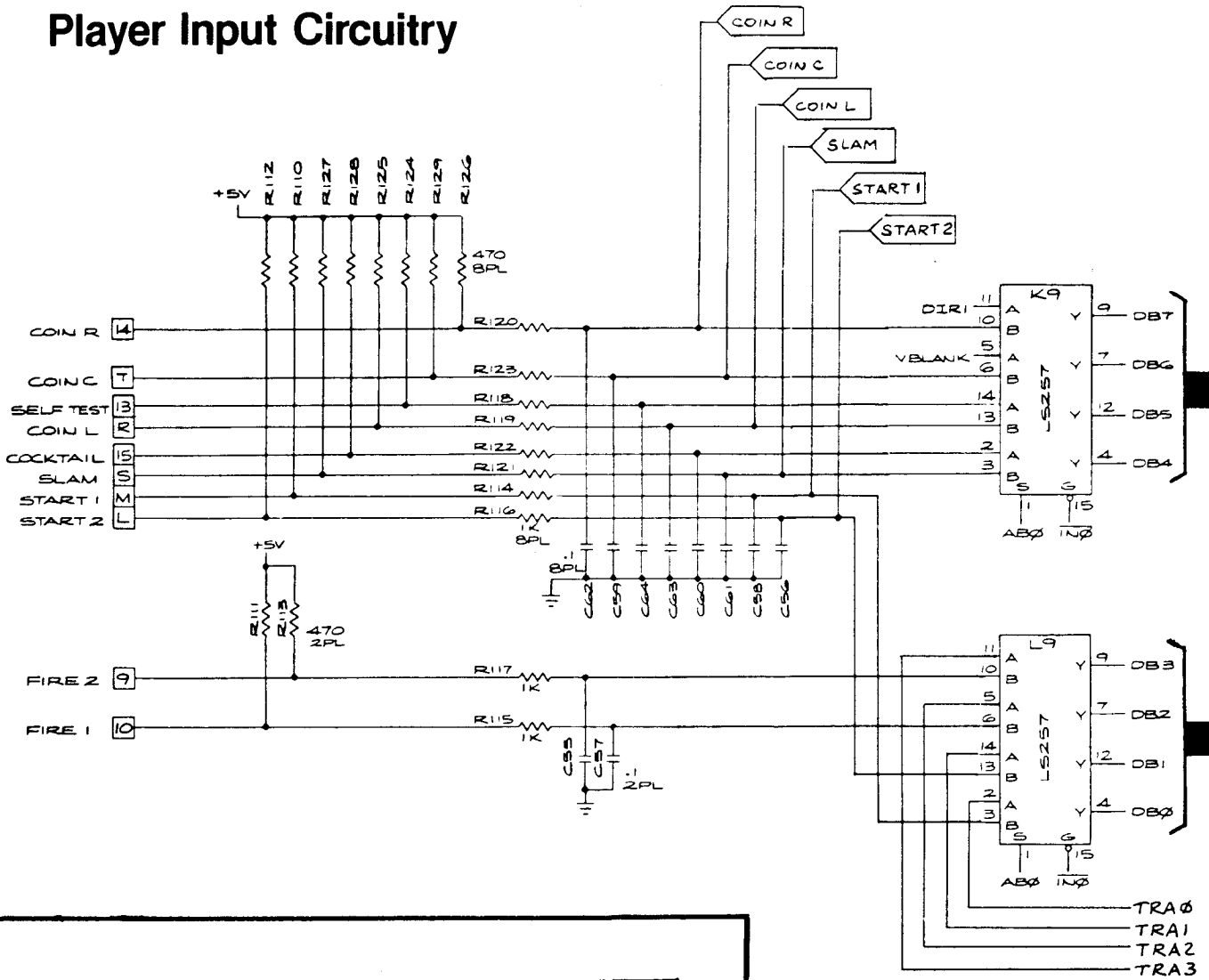
Joystick Circuitry



Option Input Circuitry

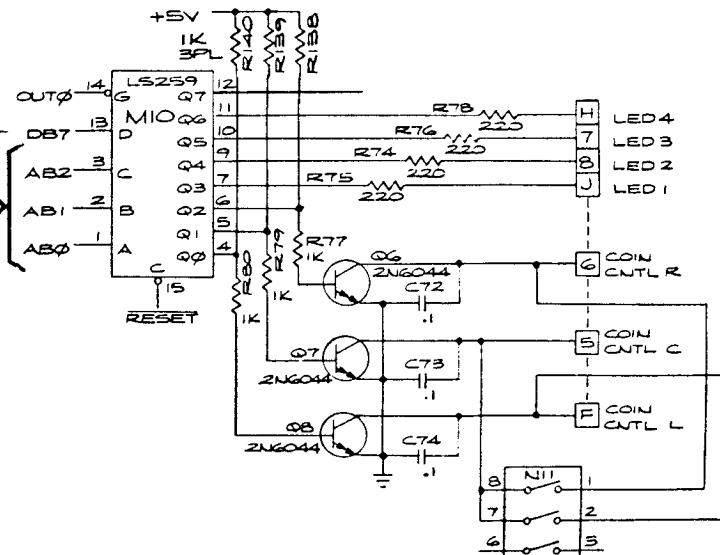


Player Input Circuitry



Coin Counter Output Circuitry

From MPU Address Bus Sheet 1, Side B



Testing the Player Inputs

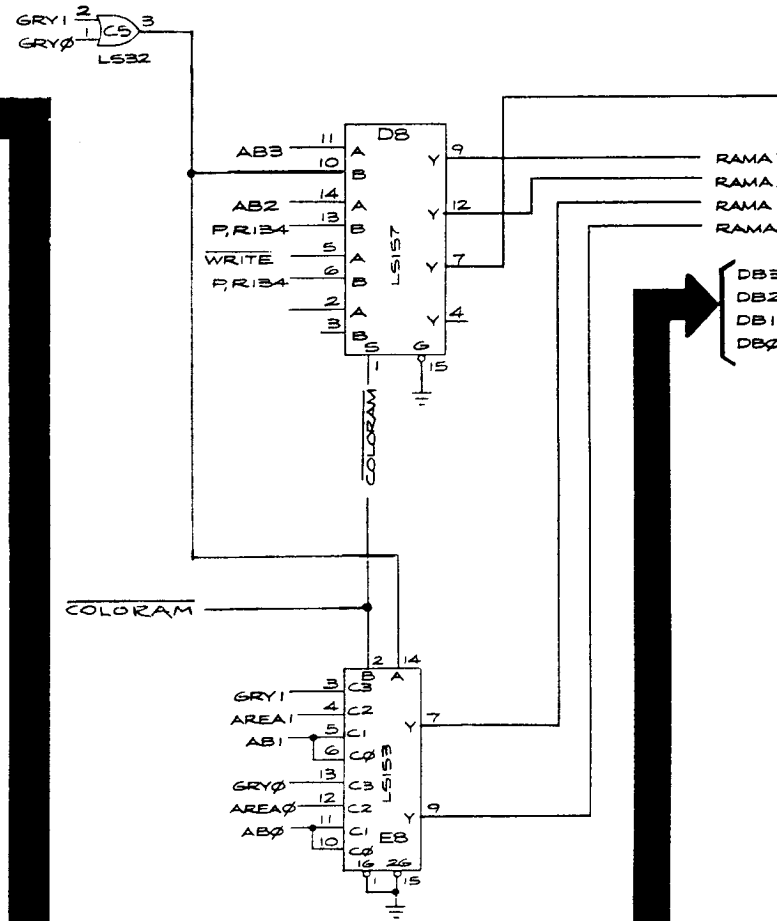
1. Perform the CAT Box Preliminary Set-up.
2. Set the CAT Box switches as follows:
 - a. DBUS SOURCE to DATA
 - b. BYTES to 1
 - c. R/W to READ
 - d. Key in address 0C00 (self-test switch only) or 0C01 (all others).
 - e. R/W MODE to STATIC
3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
 - a. Coin Right
 - b. Coin Left
 - c. SLAM
 - d. FIRE
 - e. START 1
 - f. START 2
4. The DATA DISPLAY will change if the switches are operating properly.

◀ Denotes a test point

Testing the Audio Outputs

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as follows:
 - a. DBUS SOURCE to DATA
 - b. BYTES to 1
 - c. R/W to WRITE
 - d. Key in address or press ADDRESS INCR
 - e. Press DATA SET
 - f. Key in data
 - g. Set R/W MODE to PULSE, then to OFF.
 - h. For each address, repeat sequence starting at Step d.

ADDRESS	DATA	RESULTS
100F	00	
100F	03	
1000	55	
1001	AF	Pure tone is heard from channel 1 out
1001	00	Channel 1 output is turned off.
1002	55	
1003	AF	Pure tone is heard from channel 2 out
1003	00	Channel 2 output is turned off.
1004	55	
1005	AF	Pure tone is heard from channel 3 out
1005	00	Channel 3 output is turned off.
1006	55	
1007	AF	Pure tone is heard from channel 4 out
1007	00	Channel 4 output is turned off.

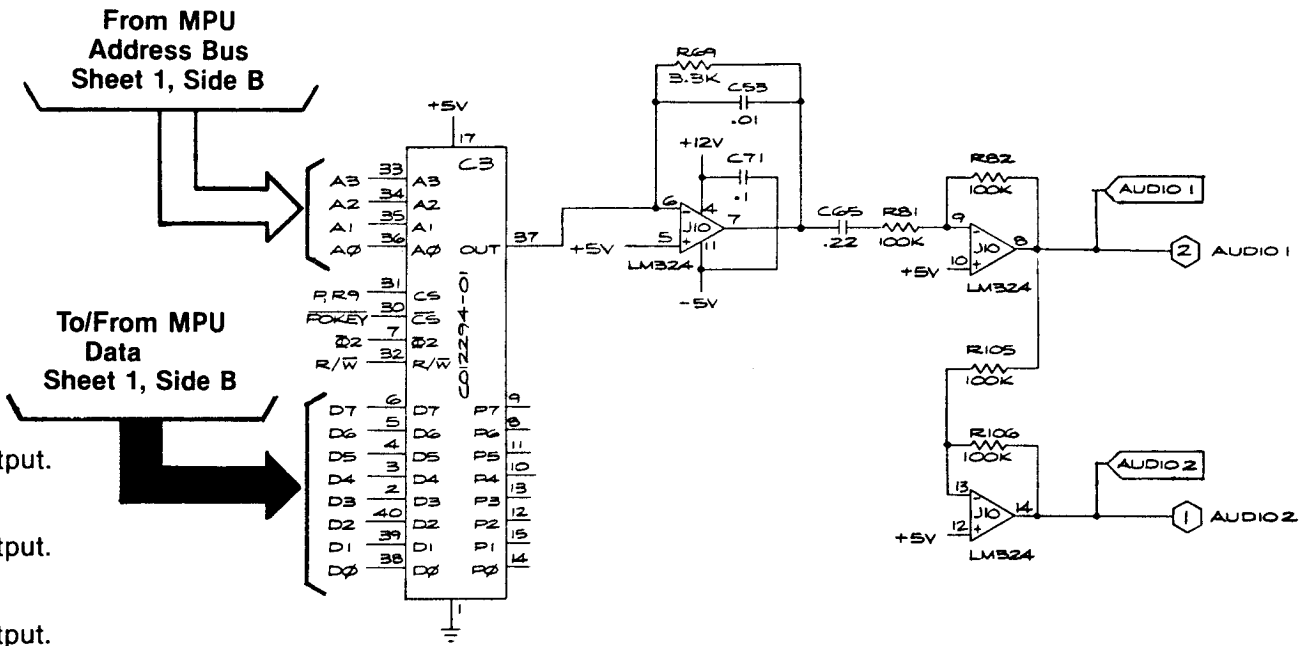


The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by E8. The output, selected by GRY0 or GRY1, is RAMA0-RAMA3 (RAM ADDRESS).

RAMA0-RAMA3 are applied to color RAM C8. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (C8 pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combinations of COLOR 1 (red), COLOR 2 (green) and COLOR 3 (blue)

Audio Output Circuitry



Channel 1 output.
off.

Channel 2 output.
off.

Channel 3 output.
off.

Channel 4 output.
off.

Video Output Circuitry

