

CINEMATRONICS, INC.
HIGH-SPEED VECTOR GAME SYSTEM
MANUAL OF ELECTRONICS

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CHAPTER 1

INTRODUCTION

The purpose of this manual is to provide a succinct and workable explanation of the operations involved in Cinematronics' general game system. Block diagrams, schematics, and a parts list are included to further this purpose. Designed around the 68000 Microprocessor, the system will be the foundation for all Cinematronics XY arcade video games in the near future. Manual inserts featuring improvements to the system and information specific to individual games will be forwarded when appropriate.

All Cinematronics games are shipped in ready-to-play condition. Each game should, however, undergo a brief inspection upon arrival. The following list may be used as a guideline:

1. Adjust the +5V DC supply to 4.8-5.1V DC.
2. Make sure all connectors, cables, and socketed ICs are seated properly.
3. Make sure that the audio and game personality modules are securely anchored with both mounting screws. Verify that standoffs are not flexing the game processor board, causing poor game personality module connection.
4. Lock the +5V DC adjustment pot in position with nail polish or a similar compound.
5. Note the game serial number for any future servicing needs.

Now, before continuing, read through the following explanations of the conventions used in this manual:

1. The heading of each major section is followed by one or more numbers in parenthesis. These numbers are schematic page and location references. The first number(s) are the page numbers. Any specific schematic location numbers and letters used are separated from the page numbers by hyphens.
2. All active-low signals are marked by minus signs after their mnemonic names.

3. Individual pin numbers referred to are separated from their IC numbers by hyphens. For example, U1-2 is the same as U1, pin 2,

CHAPTER 2

GAME PROCESSOR BOARD

TABLE 2-1: 68000 SIGNAL DESCRIPTION*

The following table lists the 68000 input and output signals, their mnemonic names, and brief descriptions of their functions.

SIGNAL	MNEMONIC	DESCRIPTION
ADDRESS BUS	A1-A23	23-bit, unidirectional, three-state bus, capable of addressing 8 megawords of data. Provides the address for bus operation during all 68000 cycles.
DATA BUS	D0-D15	The general data path. 16-bit, bidirectional, three-state bus, capable of transferring and accepting data in either word or byte length.
ASYNCHRONOUS BUS CONTROL		
Address Strobe	AS-	Indicates a valid address on the address bus.
Read/Write	R/W-	Defines the data bus transfer

as a read or write cycle.

Upper and Lower Data Strobes	UDS-, LDS-	Control the data on the data bus. When the instruction specifies a word operation, the processor accesses both bytes and asserts both data strobes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to access, then issues the data strobes required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is used. When the A0 bit equals one, the lower data strobe is used.
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Data Transfer Acknowledge	DTACK-	This input indicates to processor that data transfer is completed, causing bus cycle to be terminated.
------------------------------	--------	--

BUS ARBITRATION CONTROL CIRCUIT

Bus Request	BR-	This input indicates to processor that the Refresh Processor desires to become the bus master.
Bus Grant	BG-	This output indicates to the Refresh Processor that the processor will release bus control at the end of current bus cycle.
Bus Grant Acknowledge	BGACK-	This input indicates that the Refresh Processor has become bus master.

INTERRUPT CONTROL	IPL0- IPL1- IPL2-	These input pins indicate the encoded priority level of a device requesting interrupt. Level four is the highest priority, while level zero indicates that no interrupts are requested. The least significant bit is given in IPL0; the most significant
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is contained in IPL2.

SYSTEM CONTROL

Bus Error	BERR-	Tied high and not used. A bus error condition will be handled by the system's Watchdog Reset.
Reset and Halt	RESET-, HALT-	Applied simultaneously, these external signals cause a total system reset of the processor and external devices.

M6800 PERIPHERAL CONTROL

		Three control signals used to allow the interfacing of synchronous M6800 peripheral devices with the asynchronous MC68000.
Enable	E	The standard enable signal common to all M6800 devices. The period for this output is ten MC68000 clock periods (six clocks low; four clocks high at 800 KHz).
Valid Peripheral Address	VPA-	This input indicates that the device or region addressed is a M6800 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt.
Valid Memory Address	VMA-	This output is used to indicate to M6800 peripheral devices that there is a valid address on the address bus, and that the processor is synchronized to enable. This signal only responds to a valid peripheral address input which indicates that the peripheral is a M6800 family device.

PROCESSOR STATUS

FC0, FC1, FC2	These function code outputs indicate the state and the
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cycle type currently being executed. The information indicated by the function code outputs is valid whenever the address strobe is active. When all three outputs are high, an interrupt acknowledge cycle is being performed.

CLOCK

CLK

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input shall be a constant frequency of 8MHz.

*All information included in this table has been taken directly from: MOTOROLA DATA SHEET, MOTOROLA Semiconductor Products Inc., copyright 1982.

PART I: THEORY OF OPERATION

A. 68000 MICROPROCESSOR (1,2)

Two processors work together on the Game Processor Board: the 68000 central processor and the Refresh Processor. A standard microprocessor, the 68000 is based upon the 16-bit, 68000 microprocessor chip. A block diagram of the 68000 system's major functional units, including address and data bus buffers, is shown in Figure 1. The locations of the blocks in the diagram approximate their actual positions on the right side of the Game Processor Circuit Board. Detailed descriptions of the functions of and relations between each block and a discussion of the Refresh Processor system follow this section.

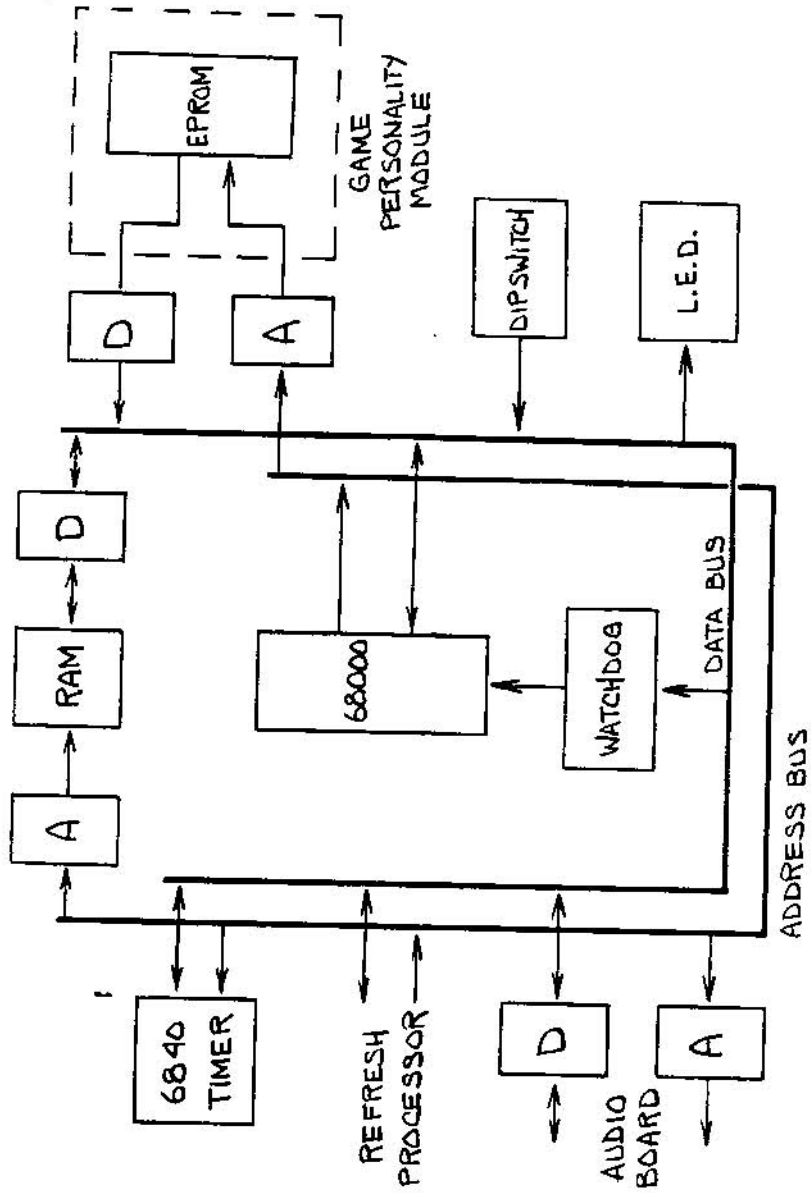
Two Programmable Array Logic circuits (PALs) are used on the Game Processor Board: U76 and U77. The PAL circuits consist of an array of AND and OR circuits, whose interconnections are programmed to provide the desired logic function of the inputs to the outputs. U76 provides primary address decoding for EPROM (OEP-) and RAM (RAMW-, OER-, RAMS-). ROMMS- is the basic decode signal for the lower portion of the 68000 memory map which includes EPROM and miscellaneous circuitry. RAMAS- is the corresponding signal for the RAM and Audio that constitute the upper portion of the memory map.

U77, the second PAL, generates the DTACK- signal required in the 68000 bus cycle operation. It determines whether or not delays need to be introduced for slow EPROMs and/or the Audio Board Interface. U77 also provides three signals used in Refresh Processor operations, QAS, QACK-, and QACK2-, along with a decode signal for the miscellaneous circuitry, MISC-. MISC- is further decoded through U74 to produce enables for the 6840 Timer (TS-), the Refresh Processor Control/Status (RPS-), the dipswitch/LED (DS-, LED-), and the Watchdog Timer. A shift register, U91, provides delays from the start of a bus cycle which are used in the generation of DTACK- and Refresh Processor signals.

B. GAME PERSONALITY MODULE (Game Personality Schematics)

The program stored in the EPROMs that make up this unit of the Game Processor Board determines the character or "personality" of the game and thus changes from game to game. There may be as many as sixteen EPROMs on the personality module, and these may be either of two types: 2732 (4K x 8) or 2764 (8K x 8).

FIGURE ONE
68000 PROCESSOR



The schematics and printed circuit layout for the Game Personality Module are for the 28-pin 2764 devices. The pinout for the 2732's is a subset of these, with the chips mounted in the lower 24 pins of the 28-pin site. The sixteen EPROMs are organized as eight pairs of 2 byte words. U1 through U8 are upper bytes, and U9 through U16 are lower bytes. The base address of the EPROM is location 0 in the system memory map.

C. RAM (3)

The RAMs on the Game Processor Board function as temporary storage and contain tables of drawing instructions. A RAM may consist of as many as ten 4016 or 6116 chips, both of which are organized as 2K x 8 bits.

The schematics and printed circuit layout for the RAMs are for 28-pin 8K X 8 devices to be used in the future. The pinout for the 4016/6616s is a subset of these, with the chips mounted in the lower 24 pins of the 28-pin site. The ten RAMs are organized as five pairs of two byte words. U7 through U11 are upper bytes, and U21 through U25 are lower bytes. The RAM base address is FFB000 hexadecimal in the memory map.

Provision has been made in some boards for battery backup of two of the RAM chips, U11 and U25, during power-down. If this option is not furnished, CR2 is replaced with a jumper, and U5 is deleted with pins 3 and 4 jumped together. In addition, BT1, R26, CR1, R25, and RP1-RP4 are deleted.

D. 6840 TIMER (3)

A programmable timer, the 6840 (U19) determines the rate of drawing by generating an interrupt at intervals of approximately twenty-five milliseconds. The 6840 has three sixteen-bit channels which are programmed through sixteen eight-bit control, status, and data registers. These registers are addressed by the three least significant processor address bits, A1-A3, and the read/write line. They are accessed on the lower data byte D0-D7. Eight of these registers may be read, and the other eight written into, by the 68000.

The base address of the eight timer registers is 40000 hexadecimal. The 6840 uses the 68000's E Clock as its input. The E Clock is one-tenth the processor's operating frequency, which is 800 KHz for an 8MHz 68000.

E. WATCHDOG RESET (2)

Sometimes referred to as the "Sanity Timer", the Watchdog Timer automatically resets the game processor in the case of system failure. The Watchdog is serviced by writing a "1" to data bit D8 at address

70000 hexadecimal. Derived from the 68000's E Clock, the time-out interval is approximately 164 milliseconds. If the Watchdog is not serviced again in that interval, a system reset is performed.

A system reset asserts the 68000 reset and halt lines to reset the 68000 and its software. It also initializes random sequential logic on the game processor and resets the Z80 Audio Board. System reset also occurs when power is first applied to the system and when the Manual Reset Switch, S2, is depressed.

F. DIPSWITCH AND LED (3)

An eight-position dipswitch, S3 provides the 68000 with game configuration input. The LED (DS1) provides output from the 68000. Its seven-segment and decimal-point display indicates various overload or error conditions. The decimal point itself is tied directly to the Watchdog Timer. See the Table 2-2 below for a list of the various LED displays and their explanations.

The dipswitch and the LED occupy the same address in the system memory map: the lower byte (D0 through D7) of location 60000 hexadecimal. The dipswitch is read, and the LED is written into, at this location. A logic "0" is an ON in both functions.

TABLE 2-2

DISPLAY	EXPLANATION
0	DRAWING OVERLOAD/AUDIO NOT READY
E	ERROR CONDITION/PROCESSOR TRAP
BLINKING DECIMAL	WATCHDOG RESET

G. INTERFACE TO THE Z80 AUDIO PROCESSOR BOARD (3)

The interface to the Z80 Audio Processor Board consists of eight bits of bidirectional data (AD8 through AD15) and eight bits of address (AA1 through AA8). Two control signals are present: an audio I/O strobe (AIOS-) to indicate valid address/data, and a read/write line (AR/W-) for data transfer direction. An interrupt (IA-) from the Audio Board to the Game Processor and a reset signal from the Game Processor to the Audio Board are also provided. The 256 byte Audio Interface is found in the upper bytes (D8 through D15) of the memory map, starting at address F8000 hexadecimal.

H. REFRESH PROCESSOR (4,5,6)

Built from discrete TTL logic, the Refresh Processor specializes in drawing, or "refreshing", the picture on the color XY monitor. A block diagram of the Refresh Processor is shown in Figure 2. The diagram illustrates the Refresh Processor system's major functional blocks in their approximate positions on the left side of the Game Processor Circuit Board.

The Refresh Processor fetches its drawing instructions from a table, or queue, in the 68000 RAM by accessing 16-bit words from the 68000 data bus. Three of the sixteen bits carry operation code, twelve carry data, and one is unused.

The three bits of operation code decode in the Instruction Decoder into the following eight operations:

- Initial X Position
- Initial Y Position
- X Drawing Rate
- Y Drawing Rate
- Color Information
- Line Length
- Control Instructions: JUMP and HALT

The twelve bits of data go onto the vector bus as an operand for the desired operation. Note, however, that the HALT operation has no operand.

The X and Y rate operations determine the slope of the line drawn by regulating the rate at which the X and Y position counters are incremented. The color information breaks down into three four-bit fields: Red, Green, and Blue. The line length operation is always last, indicating the end of the instruction sequence and triggering the circuitry to begin drawing the line. The JUMP instruction causes a jump to a specified RAM address for the next drawing instruction. When the Refresh Processor receives a HALT instruction, it sends an interrupt to the 68000 Microprocessor and ceases to draw.

Blanking is an automatic function of the Refresh Processor. There are two kinds of blanking: X/Y and Dot. If a line draws up to the edge of the monitor screen, the X and Y blanking circuitry guarantees a clean cutoff and eliminates wraparound by holding the X/Y counters in position and blanking the beam. Dot blanking prevents dots from appearing at the vertices of angles formed when two lines meet on the screen.

The X and Y DACs are 561-type, ten-bit digital to analog converters. The color DACs are three four-bit discrete digital to analog converters. The conversions are accomplished by combining digital open collector outputs in a weighted resistor network.

FIGURE TWO
REFRESH PROCESSOR

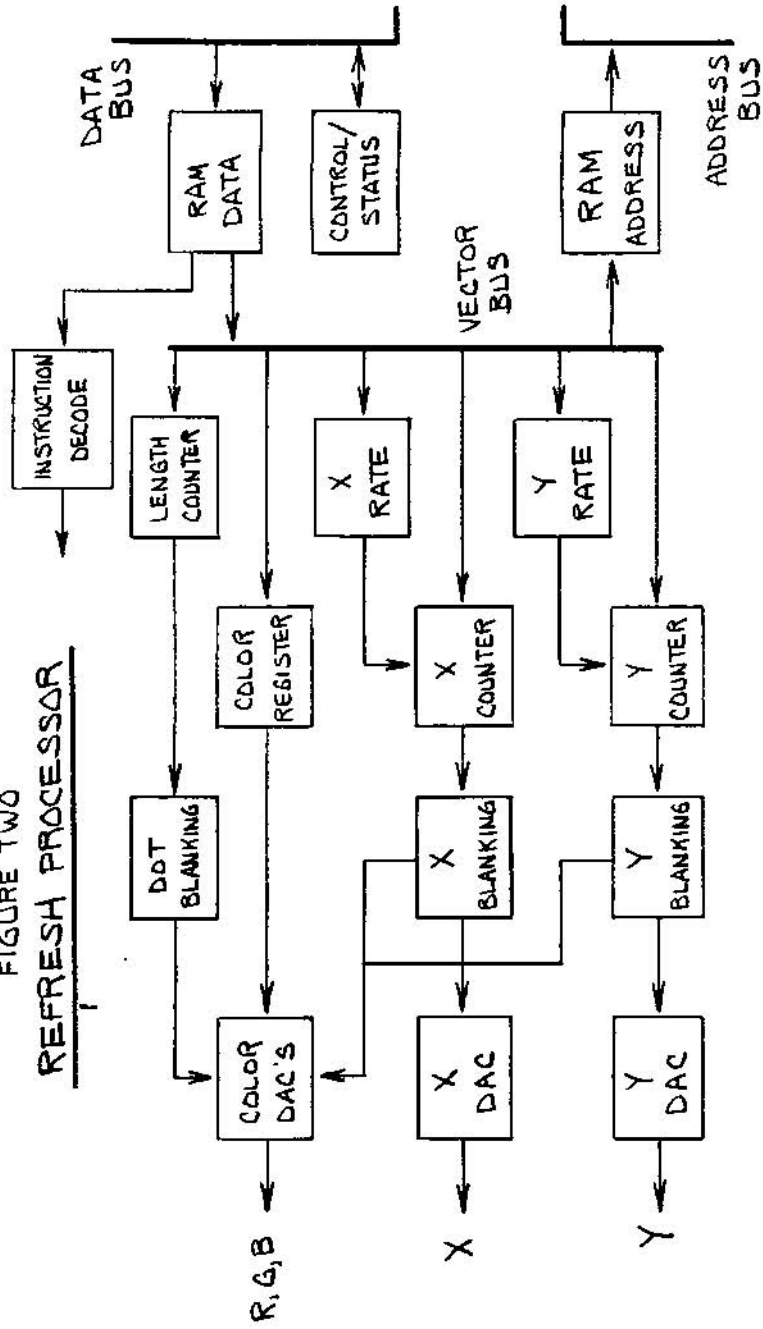


TABLE 2-3: REFRESH PROCESSOR SIGNALS

SIGNAL	MNEMONIC	DESCRIPTION
Queue Address Strobe	QAS-	Controls the address strobe signal during Refresh Processor operation.
Queue Acknowledge	QACK-	Clocks instructions into RAM data register (U59, U60) and increments RAM address counters (U85, U86, U103, U104).
Queue Acknowledge Two	QACK2-	Enables instruction decoder U53.
Refresh Processor Bus Request	RBR-	Indicates that the Refresh Processor wants to fetch an instruction from RAM.
Refresh Processor Interrupt	IR-	Indicates that the Refresh Processor is finished drawing.
Draw	DRAW-	Active when a line is being drawn.
Vector Line Length	VLNTH-	Loads length counter (U41, U42, U52) and begins drawing.
X Position	X-	Loads X position counters (U36, U48, U55).
X Drawing Rate	DELTA X	Loads rate at which the X-rate generators will operate.
Y Position	Y-	Loads Y position counters (U69, U80, U98).
Y Drawing Rate	DELTA Y	Loads rate at which the Y-rate generators will operate.
Line Color	COLOR-	Loads color registers (U32, U33).
Jump to other RAM locations	JUMP-	Loads RAM address counters with jump address.
Queue Halt	QHALT-	Stops Refresh Processor Operations.
Queue Reset	QRST-	Indicates that the Refresh Processor is not running.
Queue Start	QSTRT-	Starts Refresh Processor Operation.
Clear Queue Counter	CLQCNT-	Disables RAM address buffers

(U72, U73).

Start Drawing a Line	START-	Allows rate multipliers to increment the position counters.
Dot Blanking	DOTBLK-	Disables monitor guns while they are not drawing a line.
6MHz Clocks	6MHz A, B, C, D	Buffers clocks used throughout the Refresh Processor System.
Y Position Blanking	INT BLK Y	Indicates that the Y-beam position has gone out of bounds.
X Position Blanking	INT BLK X	Indicates that the X-beam position has gone out of bounds.
Rate Y Rate X Position up/down count for Y and X	RATY- RATX- Y UP/DN X UP/DN	Control the incrementing and decrementing of the Y and X position counters.

PART II: TROUBLESHOOTING PROCEDURES FOR THE GAME PROCESSOR BOARD

A. 68000

Put the 68000 in FREE-RUN test mode by moving the W6 jumper to the test position and removing the S1 dip jumper to disable unwanted signals. Reconnect the DTACK- signal in one of two ways: either by jumpering P4A, pins 10 and 11, or by replacing the S1 jumper with an eight-position dip switch and turning only switch 1 on. The second method lends more flexibility in testing, as it allows for individual enabling of signals. The abbreviated names of the disabled signals are printed on the circuit board next to S1.

In the FREE-RUN mode, a pseudo NO-OP is forced onto the 68000 data bus. All other devices capable of driving the data bus are disabled. While free-running, the 68000 should march through its address space, toggling the address lines along with the address and data strobes and the DTACK- line. The 68000 signals are grouped together on the P4A and P4B test connectors. Table 2-4 shows the layout of P4A, P4B, and other miscellaneous test points.

TABLE 2-4: 68000 TEST CONNECTORS

SIGNAL	PIN		SIGNAL	SIGNAL	PIN		SIGNAL
D4	1	2	D3	D5	1	2	D6
D2	3	4	D1	D7	3	4	D8
D	5	6	AS-	D9	5	6	D10
UDS-	7	8	LDS-	D11	7	8	D12
R/W-	9	10	DTACK-	D13	9	10	D14
(DTACK-)	11	12	BG-	D15	11	12	GND
(BG-)	13	14	BGACK-	GND	13	14	A23
(BGACK-)	15	16	BR-	A22	15	16	A21
(BR-)	17	18	+5VDC	+5VDC	17	18	+5VDC
+5VDC	19	20	CLK	A20	19	20	A19
GND	21	22	GND	A18	21	22	A17
HALT-	23	24	RESET-	A16	23	24	A15
VMA-	25	26	E	A14	25	26	A13
VPA-	27	28	BERR-	A12	27	28	A11
IPL2-	29	30	IPL1-	A10	29	30	A9
IPL -	31	32	FC2	A8	31	32	A7
FC1	33	34	FC	A6	33	34	A5
A1	35	36	A2				
A3	37	38	A4				
SPARE	39	40	SPARE				

NOTE: Signals in parentheses are taken on the other side of the S1 shunt.

TEST POINTS

TP1	AS-
TP2	CLK (8MHz)
TP3	6 MHz A
TP4	A23
TP5	QRST-
TP6	START-

B. REFRESH PROCESSOR

Begin by determining whether or not the Refresh Processor is running. If it is running, QRST- at test point 5 should be toggling. If QRST- is not toggling, but is low, the Refresh Processor is not running. If QRST- is not toggling, but is high, the Refresh Processor is stuck in RUN mode.

Next, check to see if the RBR signal is toggling. If it is not toggling, but is low, the Refresh Processor is not requesting the 68000 bus. If RBR is not toggling, but is high, the Refresh Processor is stuck somewhere in the 68000 bus request sequence.

If the RBR signal is working, but the Refresh Processor is still not drawing, make sure that it is not stuck at some point in the bus arbitration process by checking arbitration signals BR-, BG-, and BGACK-.

If the Refresh Processor is getting the 68000 bus, check Refresh Processor signals QAS, QACK-, and QACK2- in the Refresh Processor instruction- fetch process. All of these lines should be toggling.

If all of the lines are toggling, check Instruction Decoder U53 to see if any of the Refresh Processor registers are being loaded with instruction operands. If U53 is decoding only one type of instruction, verify that the RAM address counters are counting.

Lastly, check the X, Y, and Red, Green, and Blue outputs. If there is no X deflection, trace back through the X Position and X Rate generator circuitry. If there is no Y deflection, trace back through the corresponding Y circuitry. If there are no color outputs, trace back through the color DACs and color registers.

CHAPTER 3

Z80 AUDIO PROCESSOR BOARD

The Z80 Audio Processor Board is divided into two sections: the 68000 section and the Z80 section. An extension of the 68000's input/output system, the 68000 section is used to read the player controls and to control the Coin Counter. The Z80 section is used to generate audio and to detect coins. The two sections interact via the Command and Status Registers. Figures 3 through 5 illustrate the major functional blocks of the Z80 Audio Processor Board.

PART I: THEORY OF OPERATION FOR THE 68000 SECTION OF THE Z80 AUDIO
PROCESSOR BOARD

A. READ DECODING (5-B4)

There are eleven eight-bit readable registers on the 68000 section of the Z80 Audio Board. Each of these registers has a unique address. (See Table 3-1). The two Read Decoders, U52 and U55, decode the address from the 68000 into eleven separate select lines, one line for each of the readable registers.

When the 68000 needs to read a certain register, the two Read Decoders are first enabled by a combination of Read/Write (R/W-) high and Address Strobe low. A single Read Decoder output is then driven low, corresponding to the selected register. The data from the selected register is gated onto the local 68000 Data Bus Lines, CD8+ through CD15+, then transferred to the 68000 Board via U65. A high on Direction Control U65-1 and a low on U65-19 enable this transfer.

For an example of the above process, suppose the 68000 needs to read the STATUS HIGH register. The 68000 first sends an address word of "01" HEX to the Audio Board via U3, pins 18-32, then to Read Decoders U52 and 55. Address line AAL goes high, all other address lines low. U52-14 subsequently goes low, thereby selecting the READ STATUS HIGH register. At this time, all outputs on the other Read Decoder, U55, and on the Write Decoder, U54, are high. The data from the READ STATUS HIGH register is then transferred to the 68000 Board in the manner described above.

MAJOR SECTIONS
Z80 AUDIO BOARD

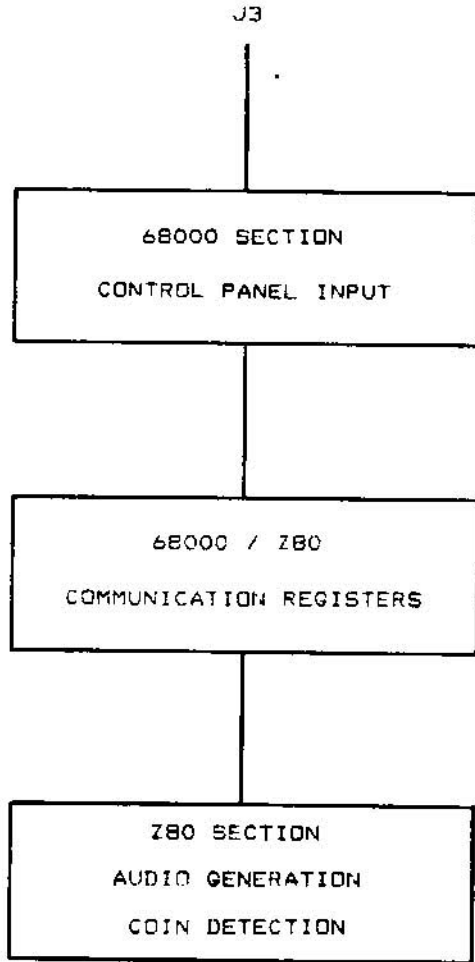
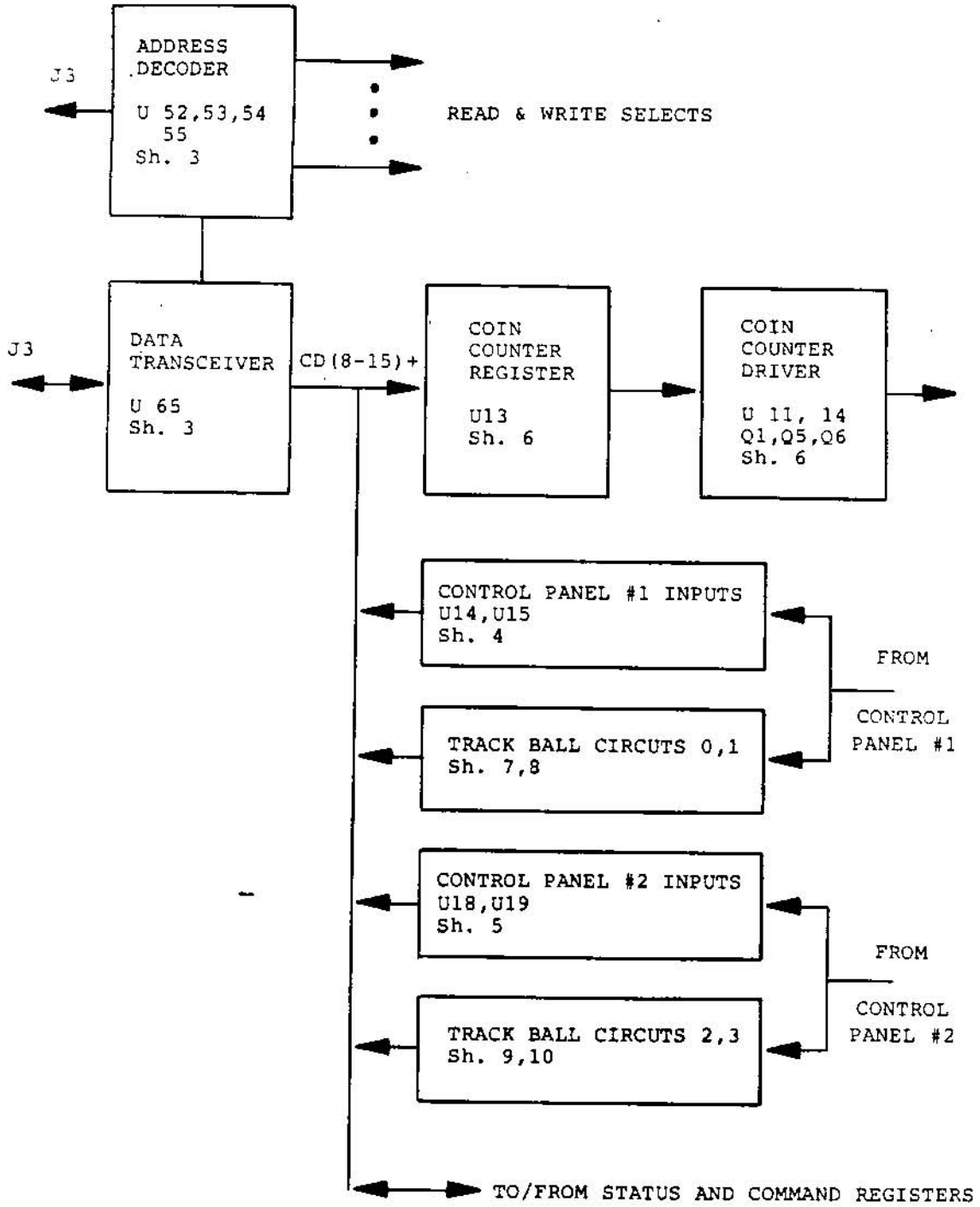
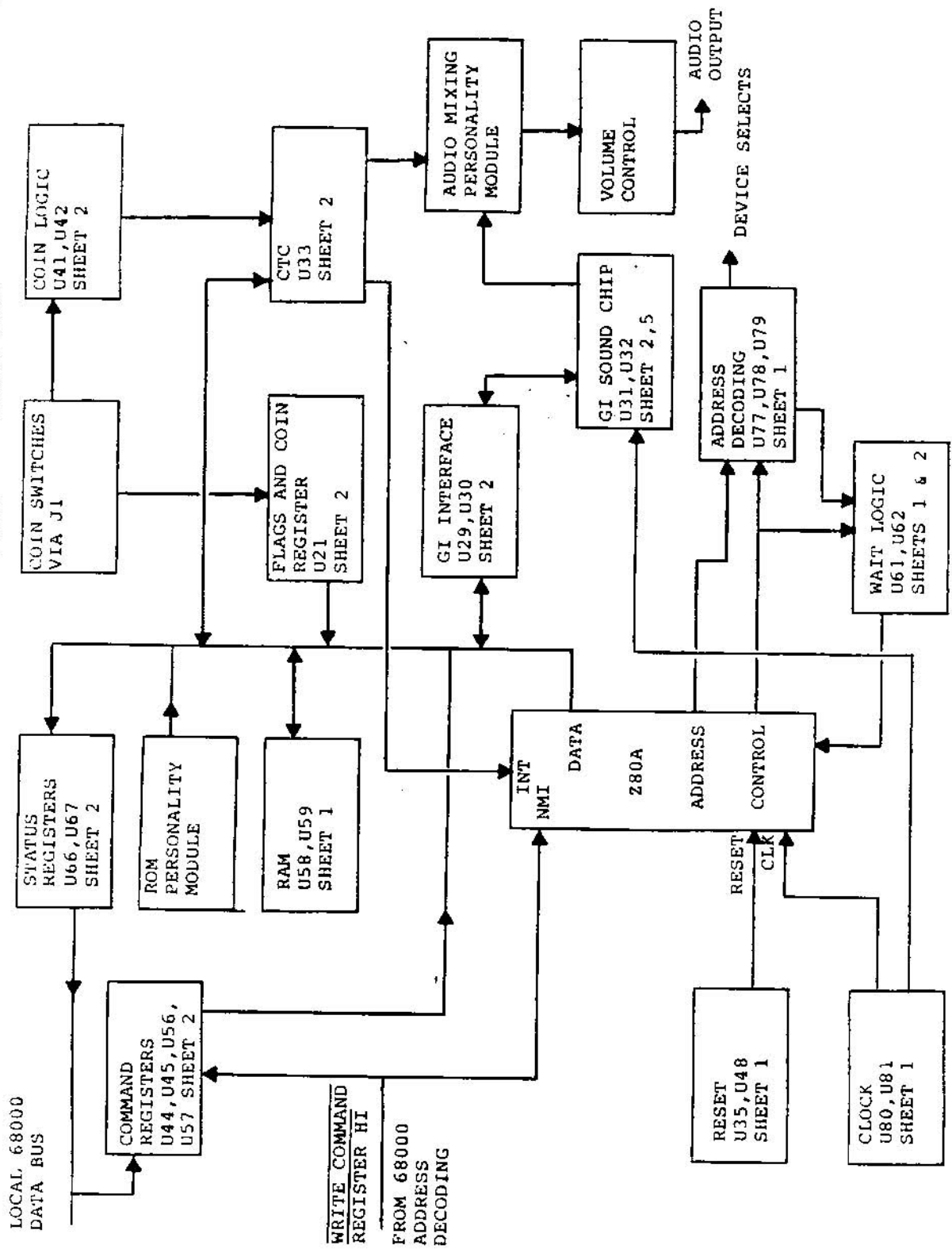


FIGURE THREE

FIGURE FOUR
 BLOCK DIAGRAM - Z80 AUDIO - 68000 SECTION



BLOCK DIAGRAM - Z80 AUDIO - Z80 SECTION - FIGURE FIVE



B. WRITE DECODING (5-C4)

The Write Decoding process is similar to that of Read Decoding. Here, there are three writeable registers. (See Table 3-2). Each of these has a unique address. The address lines from the 68000 to these registers pass through the Write Decoder, U54. In the Write Decoder, each address line is broken down into three select lines, one line for each of the three writeable registers.

When the 68000 needs to write into a certain register, U54 is enabled by a low on U54-5 R/W- and a low on U54-4. U54 then drives one of its output pins low to select one of the three output/writeable registers. The 68000 data passes via U65 to the local Data Bus lines, CD8+ through CD15+, then into the selected register. A low on U65-1 R/W- and a low on U65-19 enable this transfer.

For example of the Write Decoding process, suppose an address of "0" is selected by the 68000. All address lines are then low, causing U54-15 to go low. A write of 68000 data is strobed into the WRITE COMMAND LOW register, U56, on the Audio Board from the local 68000 Data Bus lines, CD8+ through CD15+. A high-going edge on U56-11, CAS+, enables this transfer.

NOTE: A high-going edge on the signal CAS+ is equivalent to a low-going edge on the signal AIOS, which enters the Audio Board at J3-36 from the 68000.

TABLE 3-1: 68000 READABLE REGISTERS ON THE AUDIO BOARD

ADDRESS ON LINES AA1-AA8	IC	8-BIT REGISTER	DESCRIPTION
0	U67	STATUS LOW	8-BIT DATA WORD FROM Z80 TO 68000
1	U66	STATUS HIGH	8-BIT DATA WORD FROM Z80 TO 68000
2	U27	FLAG REGISTER	SLAM FLAG, TEST SWITCHES, STATUS FULL, COMMAND FULL
3	NOT USED-----		
4	U14	CONTROL PANEL 1	8 SWITCH INPUTS (CONFIGURABLE)
5	U15	CONTROL PANEL 1	8 SWITCH INPUTS (NON-CONFIGURABLE)

6	U18	CONTROL PANEL 2	8 SWITCH INPUTS (CONFIGURABLE)
7	U19	CONTROL PANEL 2	8 SWITCH INPUTS (NON-CONFIGURABLE)
8	U17	TRACK-BALL 0	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL
9	U16	TRACK-BALL 1	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL
10	U21	TRACK-BALL 2	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL
11	U20	TRACK-BALL 3	8-BIT WORD FROM SHAFT ENCODER OR SINGLE AXIS OF TRACK-BALL

TABLE 3-2: 68000 WRITE-ABLE REGISTERS ON THE Z80 AUDIO BOARD

ADDRESS	IC	REGISTER	DESCRIPTION
0	U56	COMMAND LO	8 BIT DATA WORD FROM 68000 TO Z80
1	U44	COMMAND HI	8 BIT DATA WORD FROM 68000 TO Z80
2	U13	DRIVER REGISTER	CONTROLS COIN COUNTER AND LAMPS.

C. COIN COUNTER CIRCUIT (4-B2)

Driver register U13, one half of U11, one half of U41, one quarter of U26, Q5, Q6, and Q1 together form the Coin Counter circuit. This circuit is always reset at power-up: the reset pulse sets U11-5 high and U41-5 low, disabling the drive to the Coin Counter by guaranteeing a low at U26-3.

When driver register U13 is written into by the 68000 for the first time after reset, a low is written into U11-2, causing U11-5 to drop low, U41 to be present via U41-4, and U26-3 to go high. Driver register U13 now controls the Coin Counter.

One count of the Coin Counter is accomplished by first turning the Counter on, then off. Assuming that a "1" is written into U13-3, U13-2 goes high, causing Q5 and Q6 to turn on. The collector of Q6 is now at a potential of 1 volt or less. This low voltage causes current to be pulled through R47, thereby turning on Q1. The collector of Q1 goes from 0 volts to very near +15 volts to energize the coil in the mechanical Coin Counter. The Coin Counter is now on.

The Coin Counter de-energizes or turns off when the 68000 writes a "0" into U13-3, causing U26-3 to drop low, and Q5, Q6, and Q1 to turn off.

NOTE: Once U41-5 goes high, it stays high until reset occurs. Also, a toggling of U11-5 has no effect on the circuit's performance.

D. TRACK BALL/SHAFT ENCODER CIRCUIT (7,8)

There are four identical Shaft Encoder circuits. The following is a description of the Track-Ball 0 circuit:

Each Shaft Encoder circuit has two input-filtering networks. One of these is composed of U3, pins 8-10, U4, pins 10-11, R14-R17, CR13, and C4. The input signal to this network is differentiated by C4, then fed to U3-10 via R15. Wired as a comparator with hysteresis, U3 compares the input signal against a reference voltage of 1.75 volts generated by R1 and R2. The output of the comparator, U3-8, is in phase with the input signal. Inverter U4 supplies additional drive before the signal is sent to direction Flip Flop U5. The inputs to U5, pins 11 and 12, are approximately 90 degrees out of phase with each other. The output of the direction Flip Flop, U5-9, is high when the Shaft Encoder is turned clockwise, low when counterclockwise.

E. COUNTERS U2 and U7 (7A-3)

U2 and U7 are cascaded to form an 8-bit up/down Counter. The counting speed is determined by the rate at which clock pulses arrive at pin 14 of both IC's. The direction of the count, either increasing or decreasing, is determined by the state of the up/down input, pin 5 on both IC's. An increasing count occurs when pin 5 of both counters is low. The output of the two counters is fed to the 68000 Board when Bus Driver U17 is enabled by a low on pins 1 and 19 on U17.

F. LAMP REGISTER (4-C1)

Four bits of U13 are used as a Lamp Register. Each player panel may have as many as two LEDs installed in it. To turn on Lamp 0, the 68000 sets U13-6 high, forcing pin 12 on Lamp Driver U12 low and drawing current through R48. The other bits of the Lamp Register operate in a similar fashion.

The LED anode connects to 5 volts on the control panel, the cathode to R48 via J1-19 of the Audio Board.

Note that U12 may not be loaded in games that have no LEDs in their player panels.

G. SLAM SWITCH (4-A3)

Contact bounce at the Slam Switch on the Coin Door sets the Slam Flag. One side of the Slam Switch is connected to ground; the other enters the Audio Board via J1-J. The SLAM- signal, J1-J, is normally pulled up to +5 volts by R107. After filtering by R108 and C77, SLAM- is fed to U11-11. Assuming that the output of the SLAM FLAG+ signal U11-9 is low, any contact bounce at the Slam Switch sets the Slam Flag by causing a "1" to be clocked to U11-9.

The 68000 resets the Slam Flag by setting U13-19 first low, then high. The SLAM FLAG+ signal is sensed by the 68000 via U27-4.

H. TEST SWITCHES (4-A6)

There are three test switches on the Operator Convenience Panel. Each is furnished with a pull-up resistor on the Audio Board. The 68000 reads these switches via U27, pins 2, 15, and 17. All three switches need not be used in all games.

PART II: THEORY OF OPERATION FOR THE Z80 SECTION OF THE Z80 AUDIO
PROCESSOR BOARD

A. Z80 (I-B7)

The microprocessor used in this system is a 4 MHz Z80. All of the Z80's address, data, and control outputs are buffered by bus drivers: U70, U72, U73, and U74. These buffers are enabled when the Bus Acknowledge signal BUSAK+ is low, the normal state of BUSAK+ since jumper W11 is omitted.

B. DATA BUS DIRECTION CONTROL

A high Direction Read signal DIR RD- allows the Z80 to write into RAMs and other external devices. A low DIR RD- signal allows the transfer of data from the RAMs, ROMs, and other external devices to the Z80. The DIR RD- signal is low only under either of the following two conditions:

1. When the Z80 wishes to read data. Here, the Buffered Read signal BRD- is low at U36-9.
2. When, during interrupt-acknowledge cycles, the Z80 reads a vector address from the data bus. Here, both the BM1- and the BIORQ- signals are low at U37-1 and U37-2.

The Z80 generates sixteen address lines. After buffering, these lines are referred to as BA0+ through BA15+. BA0+ is the least significant bit. The most significant bit, BA15+, is not used.

Similarly, after buffering by data bus driver U70, the eight data bus lines are referred to as BD0+ through BD7+.

U74 buffers the following five control signals generated by the Z80:

TABLE 3-3

SIGNAL	OCCURRENCE
BM1-	BUFFERED MACHINE CYCLE 1
BMREQ-	BUFFERED MEMORY REQUEST

During instruction fetches.

When the Z80 reads or writes data from or to memory-mapped devices.

BIORQ-	BUFFERED I/O REQUEST	When the Z80 reads or writes data from or to counter timer chip U33.
BRD-	BUFFERED READ	When the Z80 reads data.
BWT-	BUFFERED WRITE	When the Z80 writes data.

U71-23, the bus acknowledge output of the Z80, is not used. The HALT- output is used to turn on the LED. The HALT- signal should normally be high. If this signal drops low, the LED illuminates, indicating a severe problem in the Z80 section of the board.

C. Z80 CONTROL LOGIC

This section describes the generation of three of the six control inputs to the Z80: Clock+, Reset-, and Wait-. The control input Bus Request (BUSRQ-) is not used. Interrupt (INT-) and Nonmaskable Interrupt (NMI-) are described in the CTC and 68000 Communication sections of this manual.

1. CLOCK CIRCUIT (3-B7)

The Clock Circuit provides the Audio Board with a stable source of timing, thus insuring, among other things, that all audio sounds remain in tune. Composed of U81, U80, Y1, and other discrete parts, the Clock Circuit consists of an oscillator and several dividers and drivers.

The oscillator is composed of U81, pins 1, 2, 8, 9, 10, and 11, Y1, R143, R144 and C133. The output of the oscillator circuit is 14.318 MHz clock at U81-2. This signal is fed into divider U80-13. Running at a fixed rate, the oscillator serves as a tuning fork for the Audio Board.

The dividers gear down the oscillator frequency by a factor of four. After first supplying 3.58 MHz to U81, pins 5 and 13, then undergoing an additional division by two, the dividers generate the clock for the GI sound chips by supplying 1.79 MHz at U80-9.

The 3.58 MHz output of divider U80-10 is used to generate SYS CLK+ and CPU CLK+. CPU CLK+ is buffered by a circuit composed of U81, pins 12 and 13, R129, R130, R133, R134, and R135. CPU CLK+ is fed to two places: to the Z80 at U71 and to the CTC at U33. Resistors 113 and 114 act as the terminator for CPU CLK+. CPU CLK+ is in phase with SYS CLK+.

The signal AUDIO CLK at U75-12 has a period of approximately 8.4 microseconds and is not used.

2. RESET CIRCUIT (3-C7)

The Reset Circuit forces the processor and other registers on the Audio Board into their proper initial states and prevents the generation of unwanted sounds. The Reset Circuit may be activated in the following two ways:

a.) Power Up:

The Power-up Reset Circuit is composed of CR4, CR5, R137-R142, C130, Q2, and U48, pins 8 and 9.

At power up, the negative side of C130 is very close to 5 volts. This causes Q2 to be turned on and the output of the circuit, U48-8, to be high. C130 now begins to charge; i.e., the voltage on its negative side goes from 5 volts down to ground. When the negative side of C130 reaches a potential of approximately .7 volts, Q2 turns off, forcing U48-8 low. To provide a clean output pulse at U48-8, R140 supplies positive feedback between U48-8 and the base of Q2. The pulse width at U48-8 is approximately 200 milliseconds.

b.) 68000 Interface:

The signal A RESET- is fed to the audio board at J3-38 and is buffered by U63, pins 4 and 16. U49 is used to "OR" together the two reset inputs. When the 68000 activates its reset line, U49-5 is forced high, U49-4 low. U49-4 is fed to Flip Flop U35 at pins 1 and 2. As long as the clear input to this Flip Flop, U35-1, is low, its output, U35-5, is low.

When the reset pulse becomes inactive, i.e., when pins 1 and 2 of U35 go high, the output of the Flip Flop, U35-5, does not go high until a positive edge is seen at U35-3. U35-5 is buffered by U75 and is fed to the CPU and the CTC. The rest of the Audio Board is reset via the system reset line SYS RESET-.

3. WAIT LOGIC (2-A1)

The Wait Logic forces the Z80 to pause under two conditions:

a.) Instruction Fetches from Memory:

Data from PROM memory is available 450 ns after the PROM has been addressed. Though fast enough for other reads of the PROM by the Z80, this speed is too slow when the Z80 is fetching instructions. Thus, U61 is used to generate a pulse which forces the Z80 to wait for the instruction words from PROM memory.

The pulse is generated in the following manner: Initially high, WM1- is fed to the Z80 via U36, pins 11 and 13. When an instruction fetch occurs, the signal BMI- goes low at U61-2. When the SYS CLR+

completes a low-to-high transition at U61, pins 3 and 11, U61-6 goes high, and U61-9 remains high. The two highs activate the signal WM1-, forcing it low.

The Wait Pulse to the processor is deactivated during the next positive transition of SYS CLK+, as U61-6 remains high and U61-9 falls low.

b.) Z80 Reads or Writes to the GI Sound Chips:

When reading or writing to GI Sound Chips U31 and U32, the Z80 must wait for two Time States, or T-States. For circuit simplicity, the signal ANY I/O-, generated by U60-6, determines when these states need to be inserted. Sometimes active for other reasons, the signal ANY I/O- is always active low whenever the GI Sound Chips are addressed.

The Wait Circuit for the GI Sound Chips is composed of U62, one half of U37, and several additional gates. Wait States during Z80 reads or writes to the GI Sound Chips are generated as follows:

The signal ANY I/O- is inverted by U49, pins 1-3. The outputs of U49 are fed to shift register U62, pins 1, 2, and 9. Low when ANY I/O- is inactive, these inputs to the shift register force all outputs of the shift register to remain low.

When a GI Sound Chip is addressed, U49-1 goes high, causing a "1" to be shifted down the outputs of the shift register. Output pins 3 and 5 of the shift register are wired to U37, pins 9 and 10. (Output pin 3 first passes through an inverter). Low for two clock cycles after the signal ANY I/O- becomes active, the output of this gate, U37-8, is fed to the Z80 via U36, pins 11 and 12.

In addition to generating a delay of two Wait States, the fourth output of the shift register shortens the Write Pulse to the GI Sound Chips. This function is implemented at U37, pins 11-13. Four clock periods after a GI sound chip is addressed, the fourth output of the shift register goes high. This signal is fed to U37-12, forcing the output, U37-11, high.

D. Z80 ADDRESS DECODING (1-C5)

Address decoding is performed by U77, U78, and U79. U79 decodes address lines 12, 13, and 14. The outputs of U79 select four different banks of Rom, two different banks of RAM, and two banks of memory-mapped I/O devices. Each of these banks is 4K long. Address decoding at U79 is enabled when Memory Request signal BMREQ- is active with a low at U79-4. It is disabled during Refresh Cycles (RFSH-) by a low at U79-6.

U77 decodes address lines 0, 5, and 6. Its outputs are used to generate Write Strokes to memory-mapped I/O devices. Also used to

decode address lines 0, 5, and 6, U78 generates Read Strobes for memory-mapped I/O devices. Address line 15 is not used.

E. PROM MEMORY (Audio Personality Schematics, 1)

Located on the Audio Personality Board, PROM Memory U1 and U2 contain the Audio program for the game. Note, however, that U2 is not always used.

F. RAM MEMORY (1-B3)

The RAM Memory stores the variables for the Audio Board. There are two blocks of RAM Memory. The first block consists of U58 and U59 on the main Z80 Audio Board and is only 1K bytes long. The chip-select for this memory block, U59-8, goes low only when the Z80 activates its Read or Write line and the signal SEL RAM 0- goes low. This function is performed at U46, pins 1-3 and U36, pins 1-3.

The second block of RAM, not used in some games, consists of U3 and U4 on the Audio Personality Board.

G. INPUT/OUTPUT

1. GI SOUND CHIPS (2-B6, 2-D6)

The GI Sound Chips, U31 and U32, generate the more complex game sounds. They are interfaced to the Z80 via U29 and U30. U30 temporarily stores data and address words being transferred from the Z80 to the Sound Chips. Whenever the Z80 writes and the signal SEL INT I/O- is low, pins 4-6 on U36 force U30-11 high, causing data from the Z80 data bus to be latched into U30.

The data retained by U30 is then placed onto the GI Sound Chips' data bus, GI D0+ through GI D7+, when U30's output enable pin, U30-1, goes low. U30-1 is controlled by the output of the D-type Flip Flop, U35-8. U35 synchronizes the output of U36-6 with the positive edges of the system clock.

U29 is used to transfer data from the GI Sound Chips back to the Z80. Its control inputs, U29-1 and U29-19, are forced low whenever either Sound Chip is being read.

Both address words and data words are written by the Z80 to the GI Sound Chips. However, only data words are read from the Sound Chips. Two control inputs on each Sound Chip control all reading and writing between the Z80 and the Sound Chips. When an address word is written into U31, the Write Address signal WGA0- falls low at U47, pins 4 and 10, forcing both control inputs, pins 18 and 20 on U31, high. In a similar fashion, the Write Data signal WGD0- at U47-5, and the Read Data signal RDG0- at U47-9 are encoded at U47 to control data

J6-55 feeds into a Volume Control Circuit consisting of one half of U8 and ten discrete parts. U8 is a multiplier. It multiplies the signal at J6-55 by the current flowing into U8-1 to produce an AC signal at U8-8. The current flowing into U8-1 is generated by passing the signal VOLUME A through R53 and R54. VOLUME A connects to the arm of the Volume Control Potentiometer on the Operator Convenience Panel via the main DC harness. The ends of the volume control are connected to ground and -15 volts. Thus, when VOLUME A is grounded, maximum current flows into U8-1, causing maximum gain to be available at U8-8. Conversely, when VOLUME A is at -15 volts, no current flows into U8-1, and no AC signal is available at U8-8. There may be, however, a small DC offset at U8-1, even at zero volume. VOLUME A enters the Audio Board at J1-M.

The output at U8-8 is amplified by U9, which also removes some of the DC offset generated by U8. U9 is wired to have a gain of approximately five for the AC component of the signal. The output at U9-6 is fed to the Audio Amplifier Board via J1-E. The Audio Amplifier Board provides power amplification to drive the speaker.

NOTE: A second, optional, Volume Control Circuit is formed by the other half of U8 and U10. Both Volume Control Circuits may be tied together or operated separately.

I. COMMUNICATION WITH THE 68000 (4-C6)

The 68000 sends commands to the Z80 via two eight-bit registers: Command Register Low and Command Register High. The Command Register Low is composed of U56 and U57. U56 is an eight-bit latch. Data from the 68000 is strobed into U56 when a positive-going edge occurs on the clock input U56-11, and the enable input U56-1 is low. The Z80 reads the data held in this latch by placing a low on U57, pins 1 and 19.

Composed of U44 and U45, the Command Register High functions similarly to the Command Register Low. The Command Register High, however, has a COMMAND REGISTER FULL+ flag which may be read at any time by the 68000 via U27, pins 8 and 12, or by the Z80 via U28, pins 9 and 11. This flag is composed of U43, pins 8-13.

At power-up, the COMMAND REGISTER FULL+ signal at U43-8 is forced to 0 by the system's reset pulse SYS RESET-, which is fed through U26, pins 11 and 12, to U43-10. When the Command Register High is written into by the 68000, a low on U43-12 clocked into U43 by a positive transition at U43-11 sets the flag. When the Z80 reads the Command Register High, U43-8 is reset to 0 by a low-going pulse on U26-13.

U43-9, the Q output of U43, is wired to the Z80's Nonmaskable Interrupt (NMI-) input to facilitate the rapid response of the Z80 to 68000 commands. The highest priority interrupt on the Z80, NMI- can never be locked out.

J. STATUS REGISTERS (4-C5)

The Z80 sends information to the 68000 via two status registers: Status Register High and Status Register Low. As with the Command Registers, the main difference in the functions of these two registers is that the Status Register High has a STATUS REGISTER FULL+ flag which may be read by either processor.

The Status Register High, U66, is written into by the Z80 when there is a low-going pulse on clock pin U66-11. To read the information held in this latch, the 68000 activates output enable pin U66-1. The STATUS REGISTER FULL+ flag, U43-5, is set when the Z80 writes data into U66 and is cleared when the 68000 reads the data in U66. The flag is also cleared during reset.

K. POWER DISTRIBUTION (9-C6)

Power supply voltages +5, +15, and -15 enter the game electronics package through J1 on the Audio Board. A diode is placed across each supply line to ground to prevent reverse polarity conditions. All three voltages are distributed to the rest of the main Audio Board and the Audio Personality Board via J6, and to the 68000 boards via J2.

CHAPTER 4

SUPPORT ELECTRONICS

PART I: AUDIO AMPLIFIER BOARD

The Audio Amplifier Board provides power amplification to the signal input from the main Audio Board. The Amplifier Board has a differential input at P2, pins 4 and 5. The composite audio signal from the Audio board arrives at P2-4. P2-5 is wired to ground at the Audio Board.

The signal arriving at P2-4 is a composite of the desired audio signals and noise. The signal arriving at P2-5 is noise only. The signal at P2-5 is subtracted from the signal at P2-4; i.e., the noise component is subtracted from the composite noise and audio signal, leaving pure audio. This process occurs as follows:

U3, an LM324, contains four operational amplifiers. One-fourth of U3, pins 5-7, is used to provide a low-impedance biasing voltage, equaling one-half of the supply voltage, to the other amplifier circuits. The signal arriving at P2-4 is coupled by C6 and RF filtered by R4, R5, and C7. It is then buffered by U3, pins 12-14. Similar operations are carried out on the signal arriving at P2-5 by U3, pins 8-10, R2, R3, C4, and C5.

A differential amplifier, composed of U3, pins 1-3, and R9-R12, subtracts the noise component at U3-8 from the composite audio signal at U3-14 to produce a pure audio signal at U3-1.

The pure audio now available at U3-1 is amplified and sent to the speaker as follows. The Audio Power Amplifier is composed of U1, U2, and many discrete components. U1 is wired as a noninverting amplifier with a gain set by R16 and R17. An inverting amplifier, U2's gain is set by R20 and R22. U1 and U2 are wired together in a bridge configuration. — Thus, for every signal excursion at U1-4, there is a signal excursion of equal magnitude but opposite direction at U2-4. The pure audio is coupled to U1-1 via R13, R14, and C11. C10 functions as an RF bypass. The input signal for U2 is obtained at the junction of R16 and R17. This signal, though very small in amplitude, is equal in phase to the signal appearing at U1-4. C16 and C24 couple the amplified audio signal to the speaker.

NOTE: Since an unregulated power supply of approximately +10 volts is fed to the Audio Amplifier Board, the power supply voltage for U3 is provided with additional filtering by R8, C9, and C3.

Note also that some games have a different power supply, one capable of supplying an unregulated 14 volts to the Amplifier Board. In these games, U2 and its associated discrete components are unnecessary and therefore not installed. Also, the speaker return is connected to P1-6 (ground) instead of P1-5.

PART II: COLOR XY MONITORS

Two different monitors may be used in the game system: the ELECTROHOME G08-105 and the WELLS-GARDNER 19K6401. These monitors are not directly interchangeable. Power requirements, harnessing and connectors, and signal levels vary between the two. The ELECTROHOME monitor requires 100 volts center-tapped AC, the WELLS-GARDNER 80 volts center-tapped AC. Use of the ELECTROHOME monitor requires the replacement of the 3.3K ohm resistors at R4, R12, and R20 on the Game Processor Board with 2.7K ohm resistors to reduce the color output signal levels. For harnessing and connector differences, refer to the system interconnection diagrams: 11-12056.

PART III: GAME HARNESESSES

There are four distinct types of harnesses in the game cabinet: AC Input Harness, Fluorescent Lamp Harness, Main DC Harness, and one or two Monitor Harnesses. The AC Input Harness consists of an AC line cord and connections to an interlock switch. This harness brings power to J1 of the power supply.

The Fluorescent Lamp Harness takes 120 volts AC from the power supply and distributes it to all fluorescent lamps in the game via J3.

The Main DC Harness distributes all of the DC power supply voltages. It also furnishes speaker connections and connects the Audio Board to the Control Panels, the Coin Door, the Operator Convenience Panel, and the Audio Amplifier.

Two different monitors used in production necessitate two different versions of monitor harnessing. All games using ELECTROHOME monitors have two Monitor Harnesses: a Monitor Power Harness and a Monitor Signal Cable. The Monitor Power Harness brings 100 volts center-tapped from J2 of the power supply to P400 of the monitor. A frame ground is also cabled in this harness. The Monitor Signal Cable feeds video signals generated at P2 of the Game Processor Board to P100 of the monitor.

All games using the WELLS-GARDNER monitor have only one Monitor Harness. Through this harness, J2 of the power supply furnishes 80 volts center-tapped AC filament voltage and a frame ground to P100 of

the monitor. The harness also feeds to P100 the Red, Green, and Blue signals generated at P2 of the Game Processor Board. And lastly, the harness feeds the X and Y deflection signals generated by the Game Processor Board to P200 of the monitor.

NOTE: Since there is no grounding strap in the game, all frame grounds are connected within the various harnesses.

Also, two ribbon cables are used. One 34-pin ribbon cable routes power from J2 of the Audio Board to P1 of the Game Processor Board, and one 40-pin passes communication signals between P3 of the Game Processor Board and J3 of the Audio Board.

PART IV: POWER SUPPLY

The Power Supply Plate Assembly is composed of five modules:

1. Audio Amplifier Board
2. Unregulated DC Power Supply
3. +15 and -15 Regulator Board
4. 5 volts DC Power Supply
5. Monitor Power Transformer(s)

Line voltage is routed from J1 of the Power Supply Plate to the Unregulated DC Supply, to the Regulated DC supply, and to the Monitor Transformers. Each of these assemblies has its own line fuse.

The Monitor Transformer(s) supply 100 volts center-tapped to the monitor through J2 of the Power Supply Plate Assembly. The outputs of the 5 volt DC Power Supply and the +15 and -15 Regulator Board are routed directly to the Audio Board via J4 of the Power Supply Plate Assembly. The Unregulated Power Supply provides unregulated +25 and -25 volts DC to the +15 and -15 Regulator Board, and generates +10 volts DC for the Audio Amplifier Board.

The Audio Amplifier Board receives its input from the Audio Board through the main wiring harness and J4 of the Power Supply Plate Assembly. The output of the Audio Amplifier is routed through J4 and the main wiring harness to the speaker.

The fluorescent lamp frame ground is obtained via a SPADE LUG connectd to the frame ground terminal block. 110 volts AC are fed to the fluorescent lamps through J2 of the 5 volt DC Power Supply. Note that this connection is referred to as J3 of the Power Supply Plate Assembly.

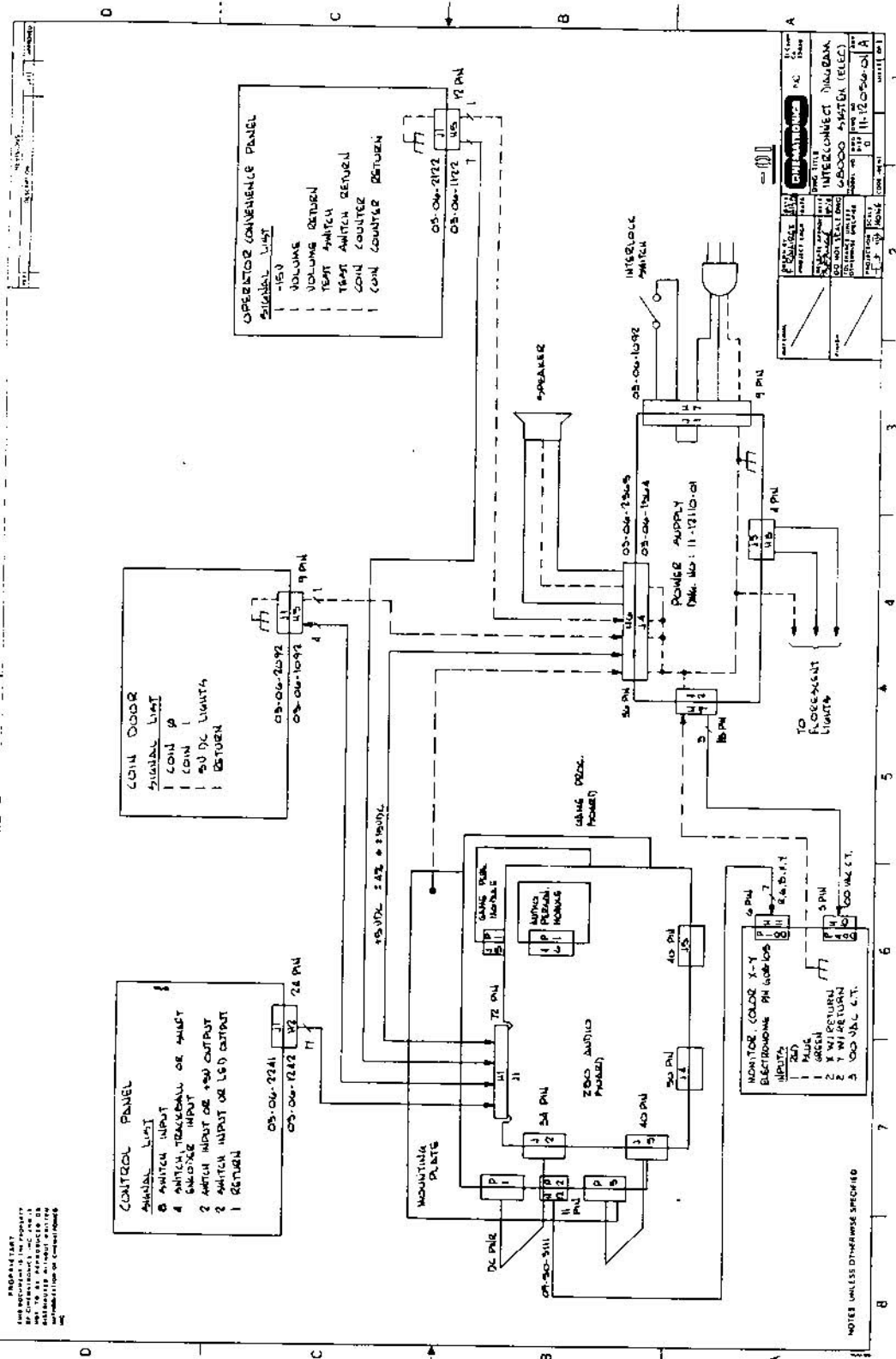
HIGH-SPEED VECTOR GAME SYSTEM
MANUAL OF ELECTRONICS

APPENDIX B

SCHEMATICS AND INTERCONNECT DIAGRAMS

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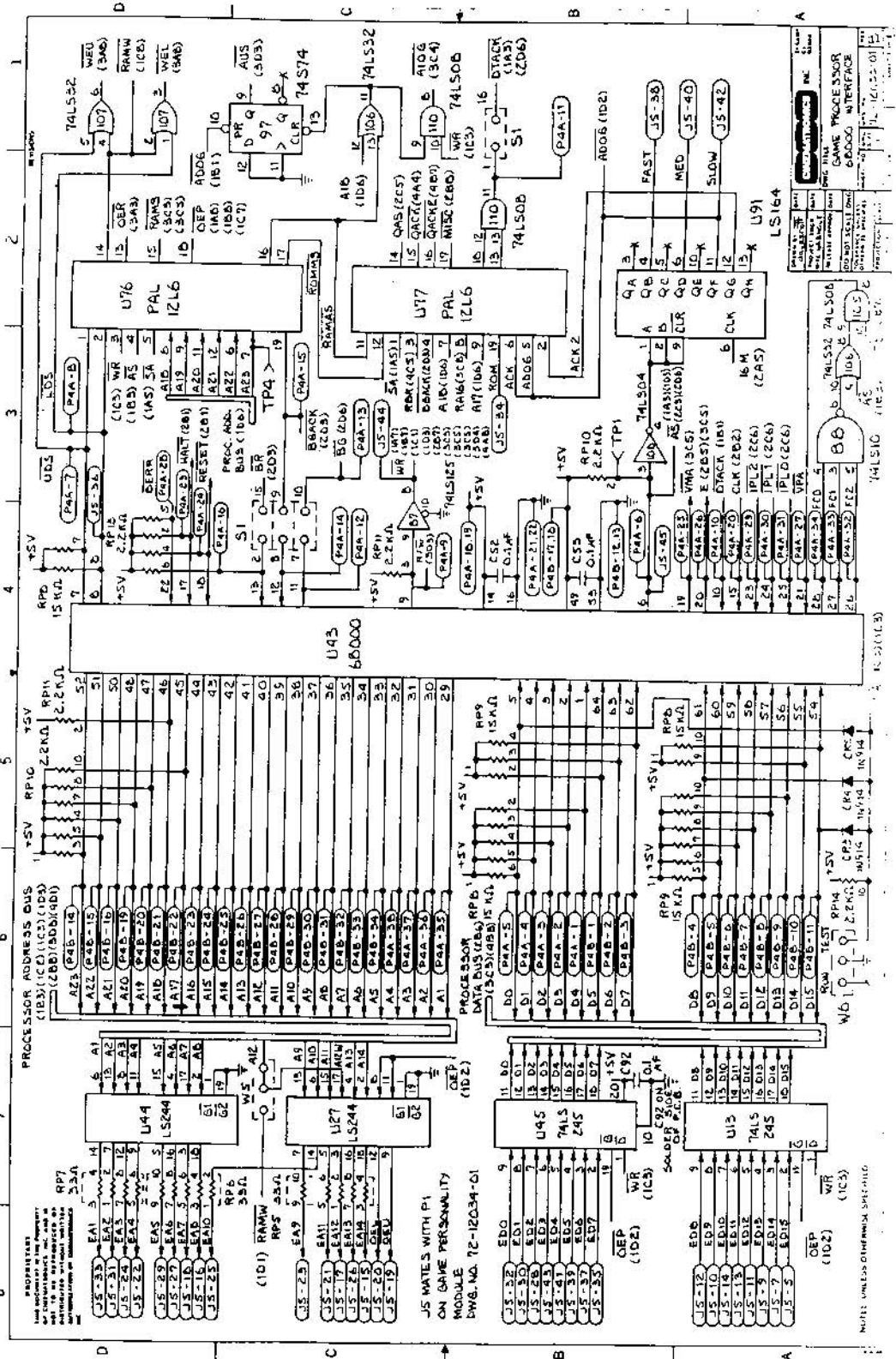


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1	INITIAL ISSUE	11-12-54		
2	REVISION			
3	REVISION			
4	REVISION			
5	REVISION			
6	REVISION			
7	REVISION			
8	REVISION			

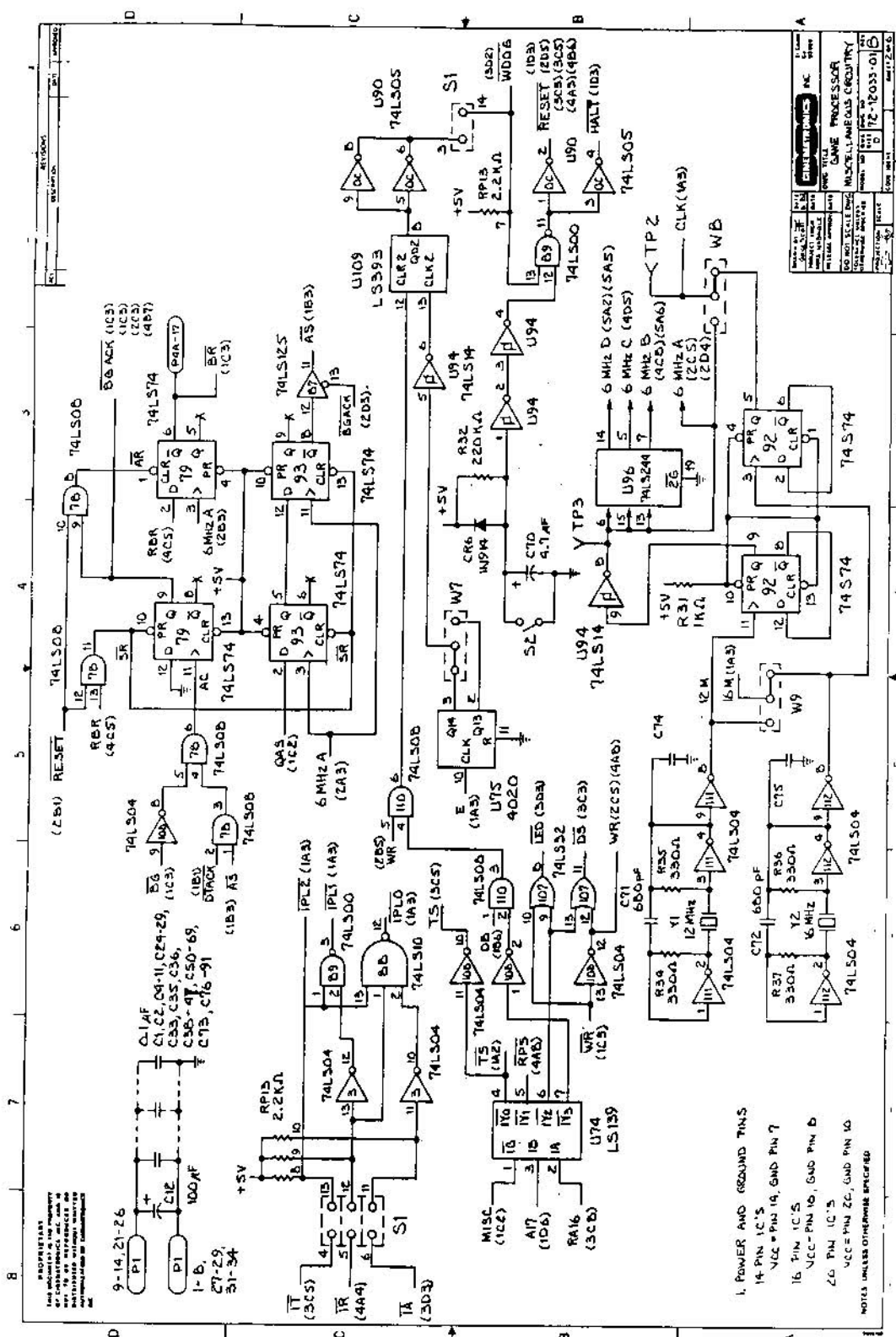
OPERATIONAL
 PROJECT TITLE: INTERCONNECT DIAGRAM
 GPO:O SYSTEM (ELEC)
 DRAWING NO.: 11-12110-01
 SHEET NO.: 1 OF 1
 PROJECT NO.: 11-12110-01
 DATE: 11-12-54



NOTE: UNLESS OTHERWISE SPECIFIED

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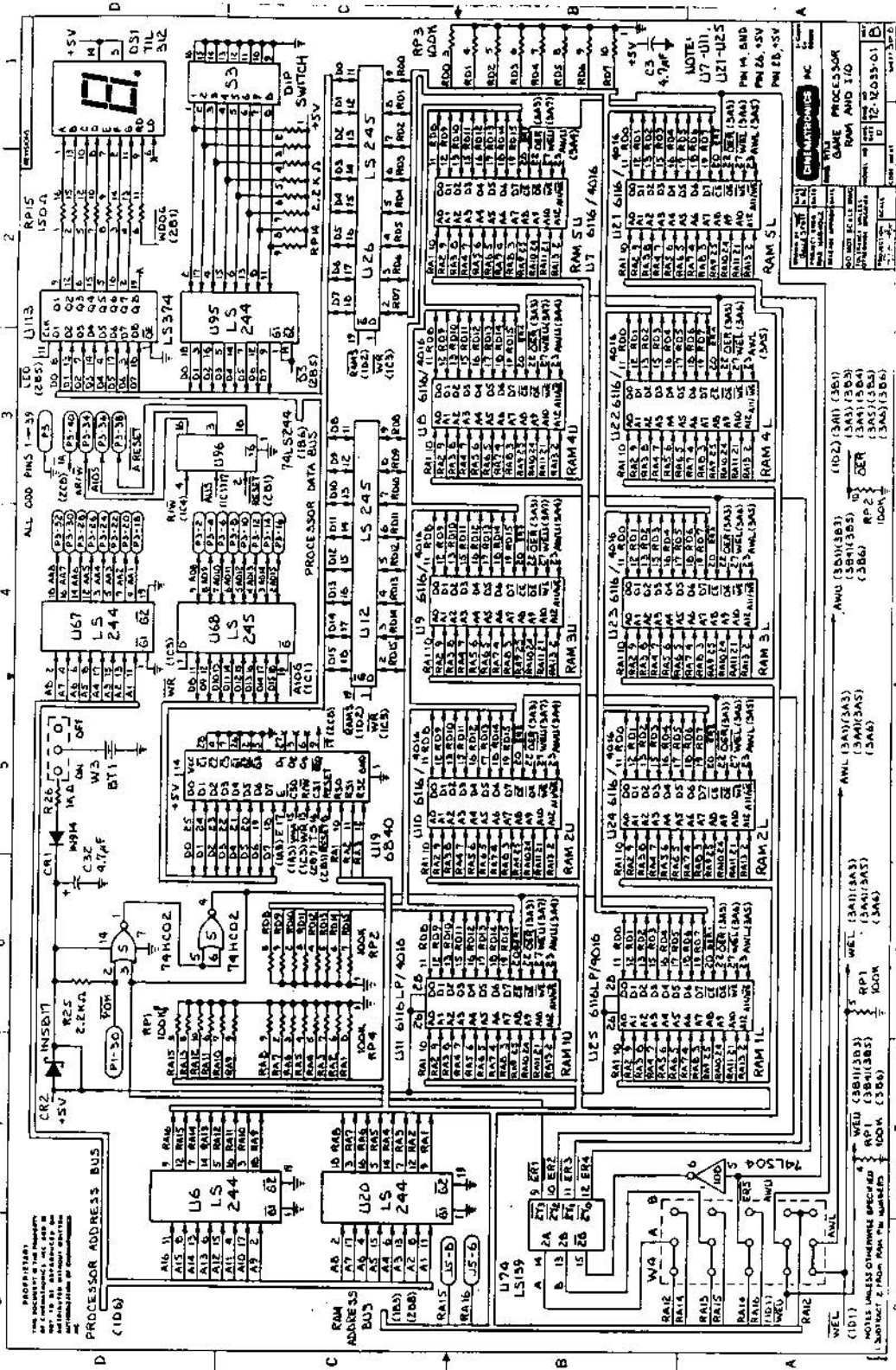
10-201013



1. POWER AND GROUND PINS
 14 PIN IC'S
 VCC = PIN 19, GND PIN 7
 16 PIN IC'S
 VCC = PIN 16, GND PIN 8
 20 PIN IC'S
 VCC = PIN 20, GND PIN 10

NOTES UNLESS OTHERWISE SPECIFIED

DATE	REV	BY	CHK
12-10-83	01
PROJECT TITLE: GAME PROCESSOR DRAWN BY: ... CHECKED BY: ... APPROVED BY: ... DATE: 12-10-83			



CHROMATRONICS

MC	1000
RAM	1000
RAM AND I/O	1000
GAME PROCESSOR	1000

RAM 1	RAM 1	RAM 1
RAM 2	RAM 2	RAM 2
RAM 3	RAM 3	RAM 3
RAM 4	RAM 4	RAM 4
RAM 5	RAM 5	RAM 5
RAM 6	RAM 6	RAM 6
RAM 7	RAM 7	RAM 7
RAM 8	RAM 8	RAM 8
RAM 9	RAM 9	RAM 9
RAM 10	RAM 10	RAM 10
RAM 11	RAM 11	RAM 11

RAM 1	RAM 1	RAM 1
RAM 2	RAM 2	RAM 2
RAM 3	RAM 3	RAM 3
RAM 4	RAM 4	RAM 4
RAM 5	RAM 5	RAM 5
RAM 6	RAM 6	RAM 6
RAM 7	RAM 7	RAM 7
RAM 8	RAM 8	RAM 8
RAM 9	RAM 9	RAM 9
RAM 10	RAM 10	RAM 10
RAM 11	RAM 11	RAM 11

RAM 1	RAM 1	RAM 1
RAM 2	RAM 2	RAM 2
RAM 3	RAM 3	RAM 3
RAM 4	RAM 4	RAM 4
RAM 5	RAM 5	RAM 5
RAM 6	RAM 6	RAM 6
RAM 7	RAM 7	RAM 7
RAM 8	RAM 8	RAM 8
RAM 9	RAM 9	RAM 9
RAM 10	RAM 10	RAM 10
RAM 11	RAM 11	RAM 11

RAM 1	RAM 1	RAM 1
RAM 2	RAM 2	RAM 2
RAM 3	RAM 3	RAM 3
RAM 4	RAM 4	RAM 4
RAM 5	RAM 5	RAM 5
RAM 6	RAM 6	RAM 6
RAM 7	RAM 7	RAM 7
RAM 8	RAM 8	RAM 8
RAM 9	RAM 9	RAM 9
RAM 10	RAM 10	RAM 10
RAM 11	RAM 11	RAM 11

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(101) WEL (381)(383) (384)(385) (386) RP2 100K (387)(388) (389)(390) (391)(392) (393)(394) (395)(396)

(102) (3A1)(3B1) (3B2)(3B3) (3B4)(3B5) (3B6) RP2 100K (3B7)(3B8) (3B9)(3C0)

WEL (3A1)(3A3) (3A4)(3A5) (3A6) RP1 100K (3B1)(3B3) (3B4)(3B5) (3A6) RP1 100K (3B6)

WEL (3B1)(3B3) (3B4)(3B5) (3A6) RP1 100K (3B6) WEL (3B1)(3B3) (3B4)(3B5) (3A6) RP1 100K (3B6)

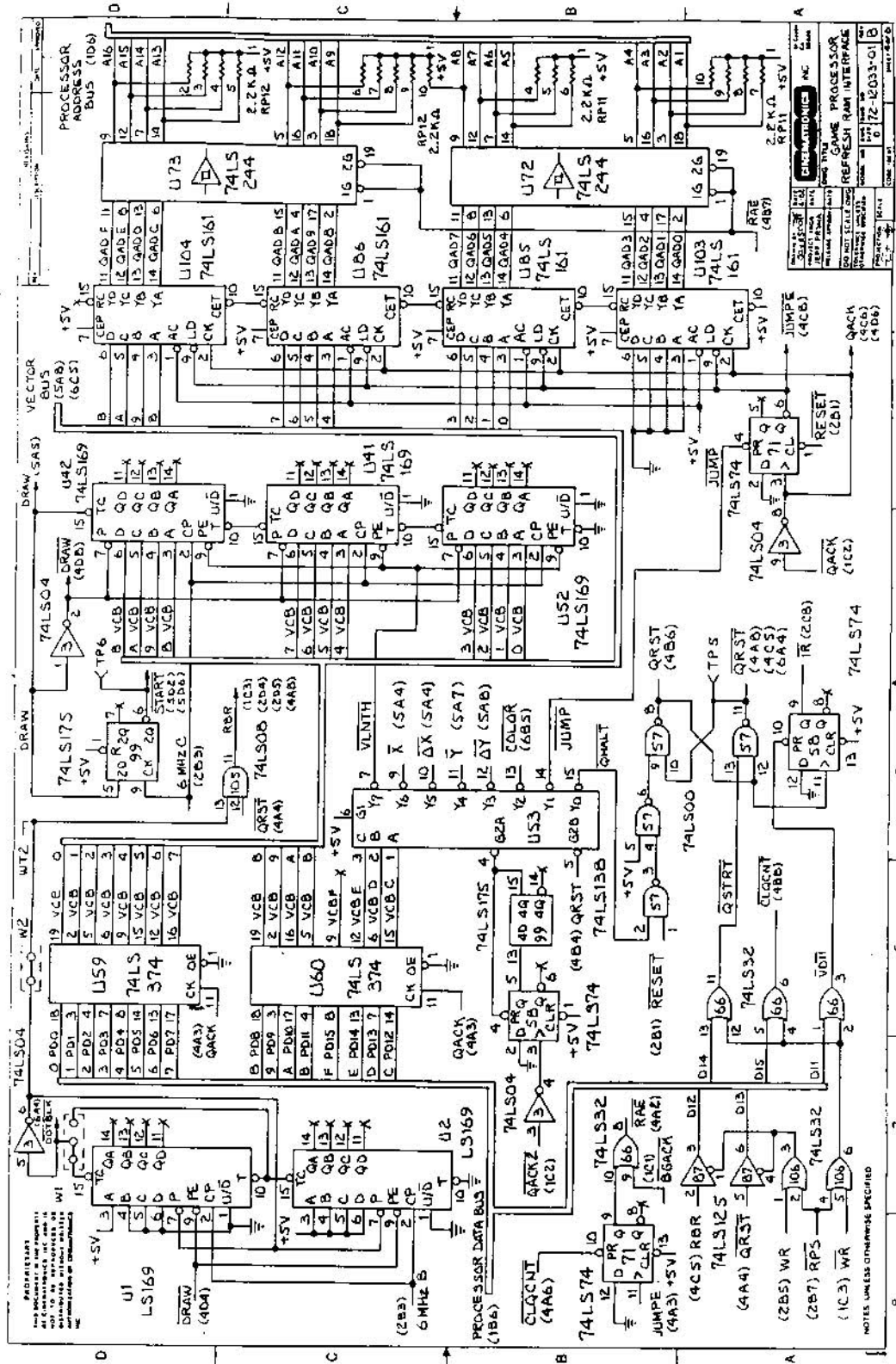
NOTE: U17-U11, U17-U12, PM 14 AND PM 25 +5V PM 15 AND PM 16 +5V

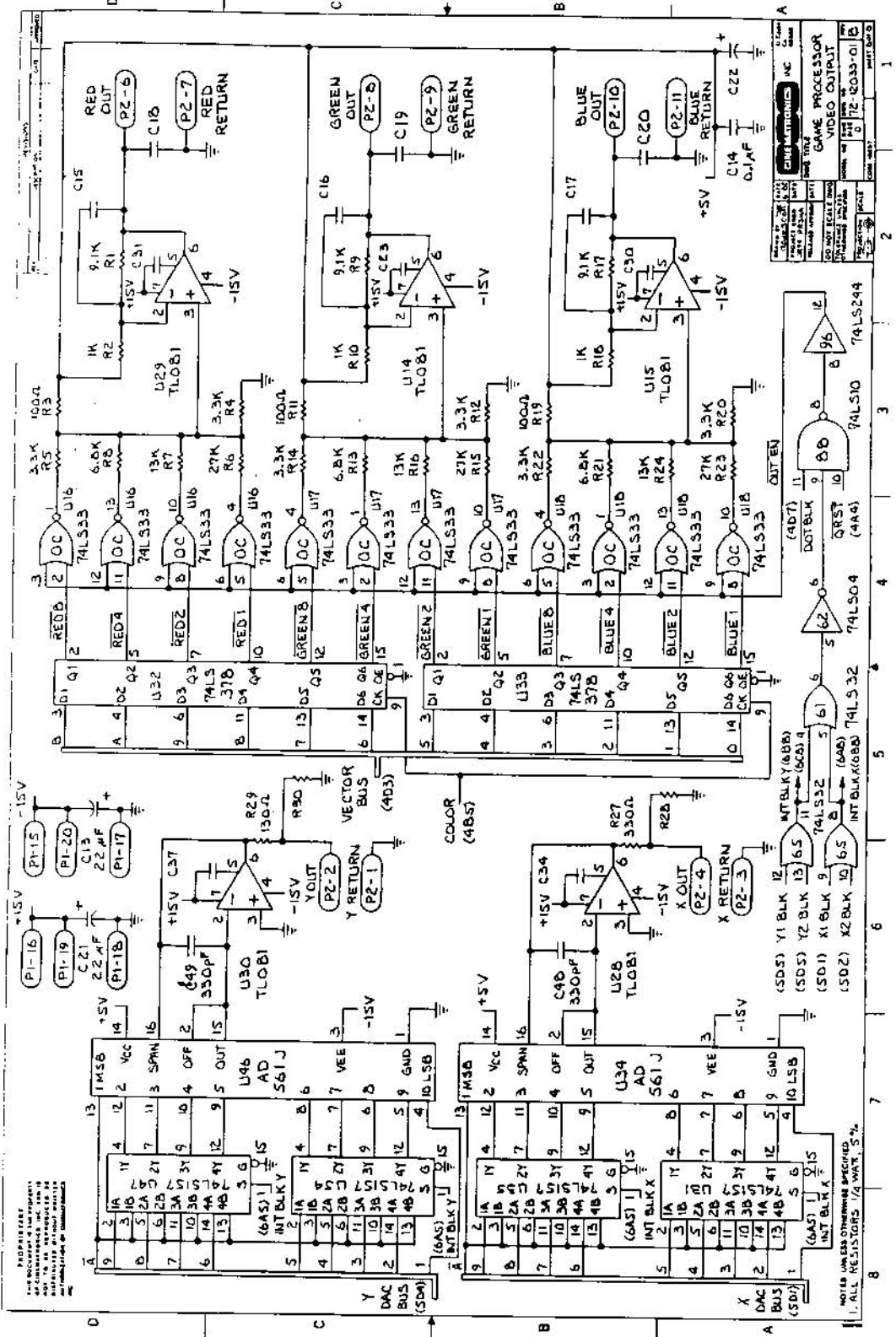
RAM 1 U17 6116 / 4016 RAM 2 U18 6116 / 4016 RAM 3 U19 6116 / 4016 RAM 4 U20 6116 / 4016 RAM 5 U21 6116 / 4016 RAM 6 U22 6116 / 4016 RAM 7 U23 6116 / 4016 RAM 8 U24 6116 / 4016 RAM 9 U25 6116 / 4016 RAM 10 U26 6116 / 4016 RAM 11 U27 6116 / 4016

RAM 1 U28 6116 / 4016 RAM 2 U29 6116 / 4016 RAM 3 U30 6116 / 4016 RAM 4 U31 6116 / 4016 RAM 5 U32 6116 / 4016 RAM 6 U33 6116 / 4016 RAM 7 U34 6116 / 4016 RAM 8 U35 6116 / 4016 RAM 9 U36 6116 / 4016 RAM 10 U37 6116 / 4016 RAM 11 U38 6116 / 4016

RAM 1 U39 6116 / 4016 RAM 2 U40 6116 / 4016 RAM 3 U41 6116 / 4016 RAM 4 U42 6116 / 4016 RAM 5 U43 6116 / 4016 RAM 6 U44 6116 / 4016 RAM 7 U45 6116 / 4016 RAM 8 U46 6116 / 4016 RAM 9 U47 6116 / 4016 RAM 10 U48 6116 / 4016 RAM 11 U49 6116 / 4016

RAM 1 U50 6116 / 4016 RAM 2 U51 6116 / 4016 RAM 3 U52 6116 / 4016 RAM 4 U53 6116 / 4016 RAM 5 U54 6116 / 4016 RAM 6 U55 6116 / 4016 RAM 7 U56 6116 / 4016 RAM 8 U57 6116 / 4016 RAM 9 U58 6116 / 4016 RAM 10 U59 6116 / 4016 RAM 11 U60 6116 / 4016

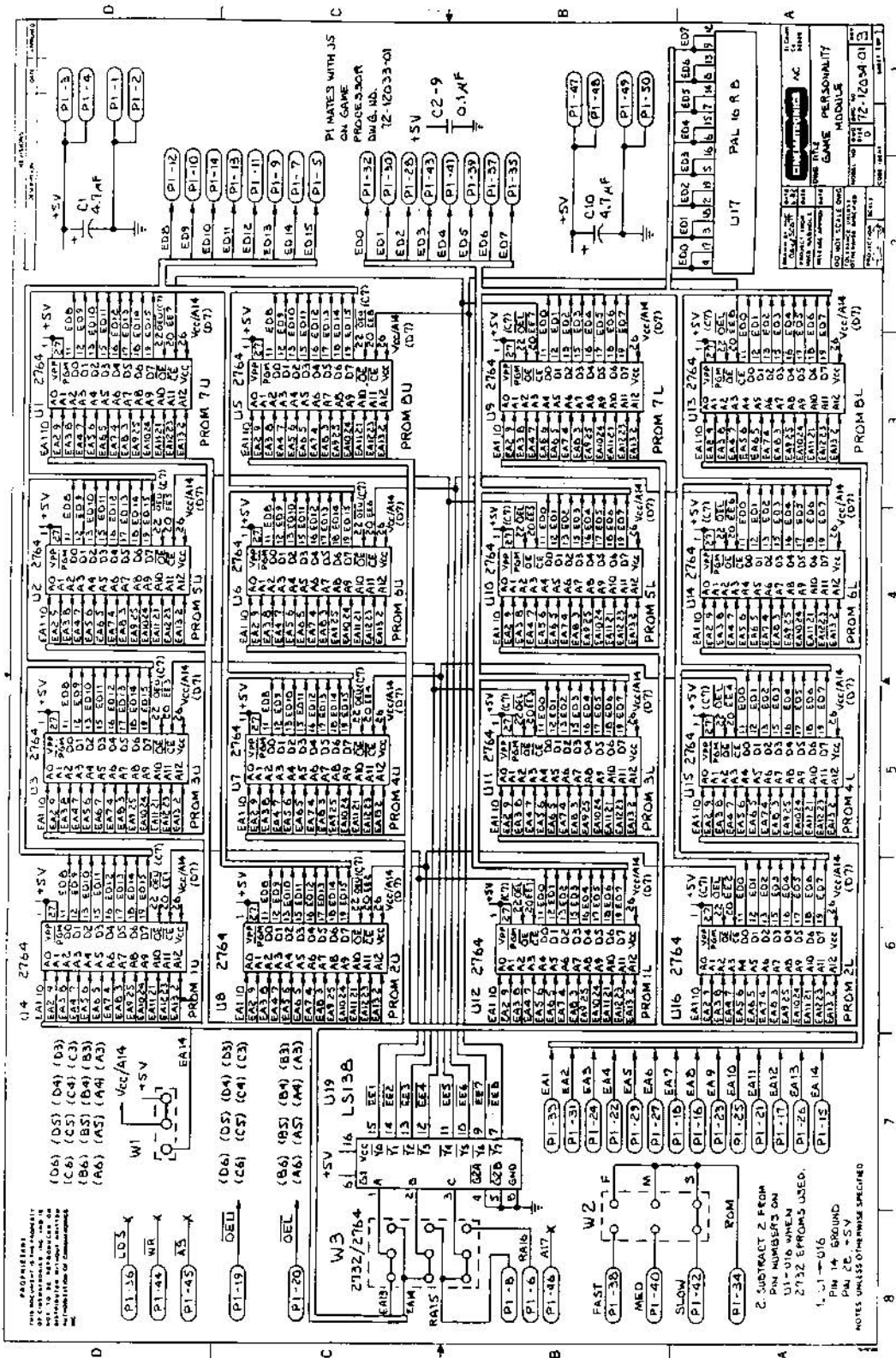




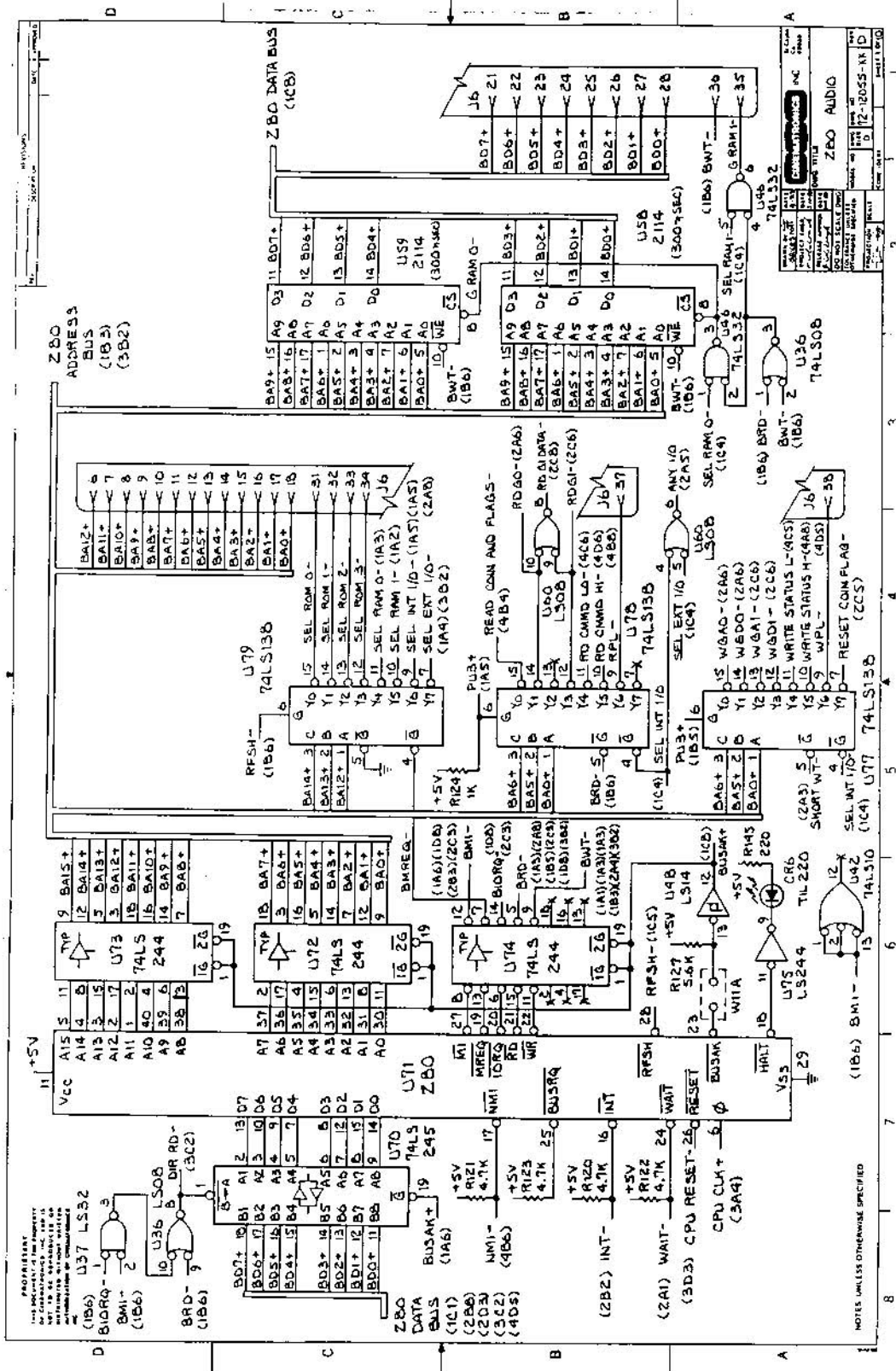
74LS33		74LS10		74LS20		74LS15		74LS13		74LS14		74LS19		74LS32		74LS04			
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol

NOTES UNLESS OTHERWISE SPECIFIED:
 1. ALL RESISTORS 1/4 WATT, 5%

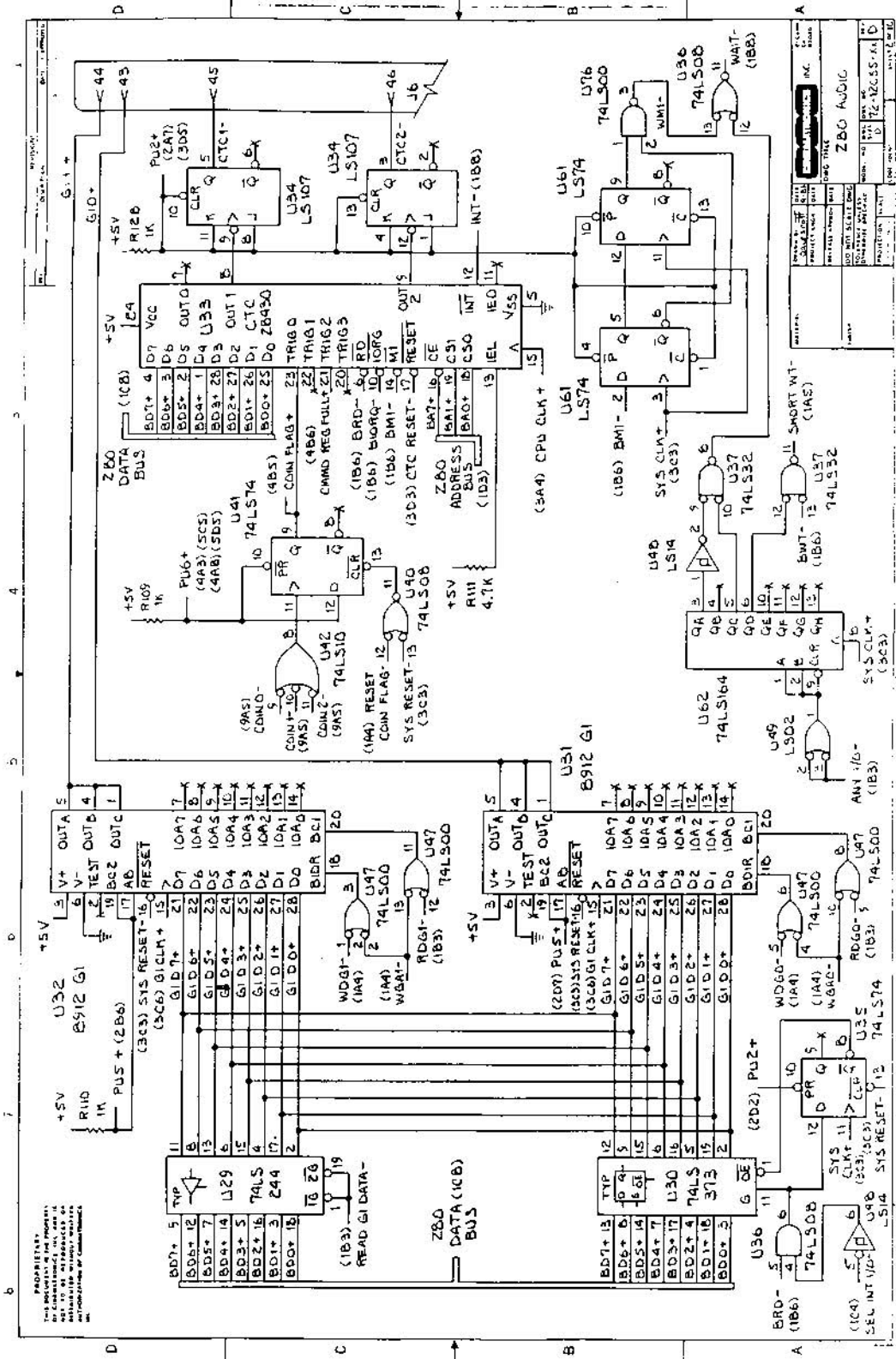
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 DATE 08-28-2014 BY 60322
 AUTHORITY 33 CFR 117.02

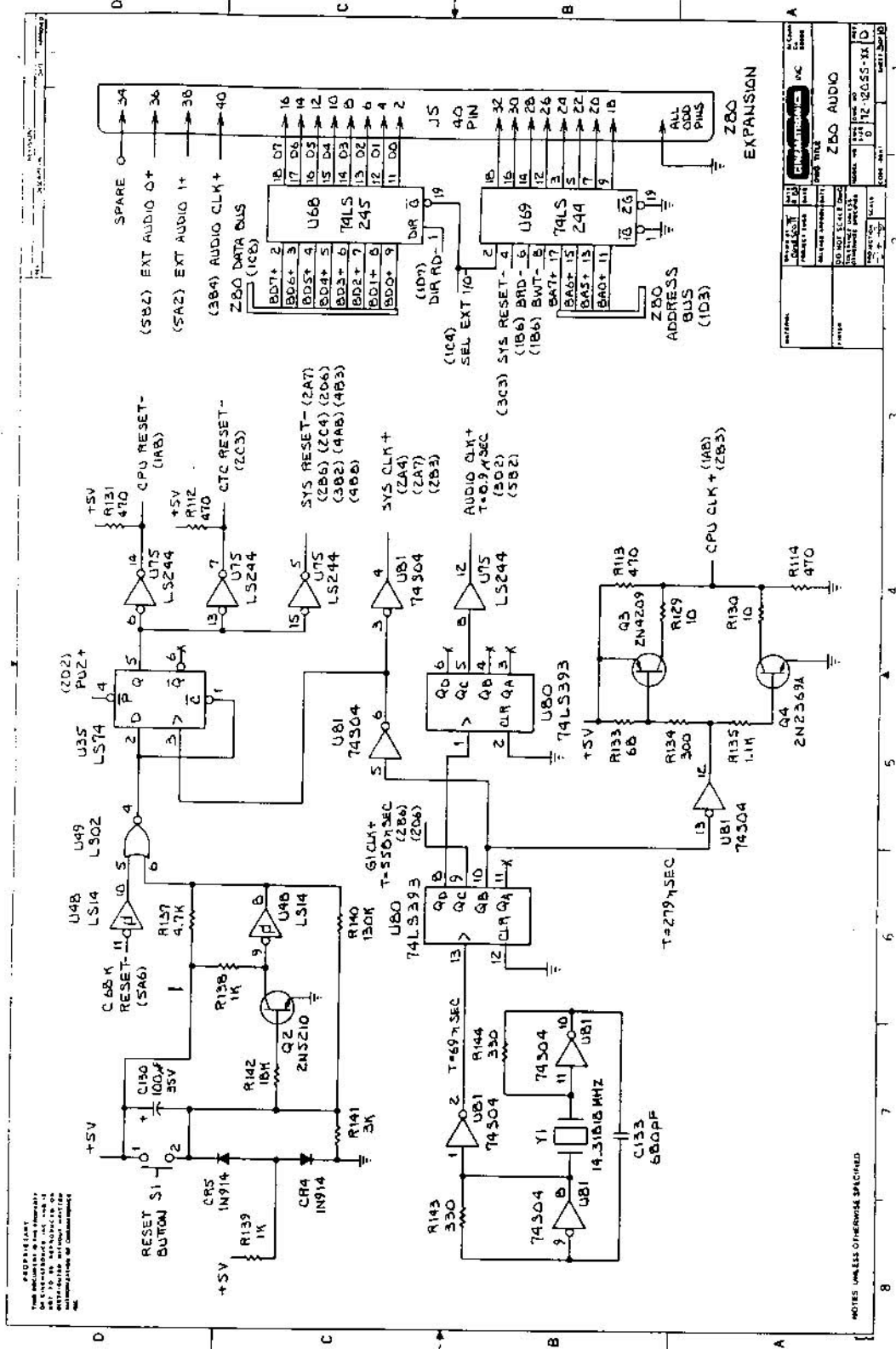


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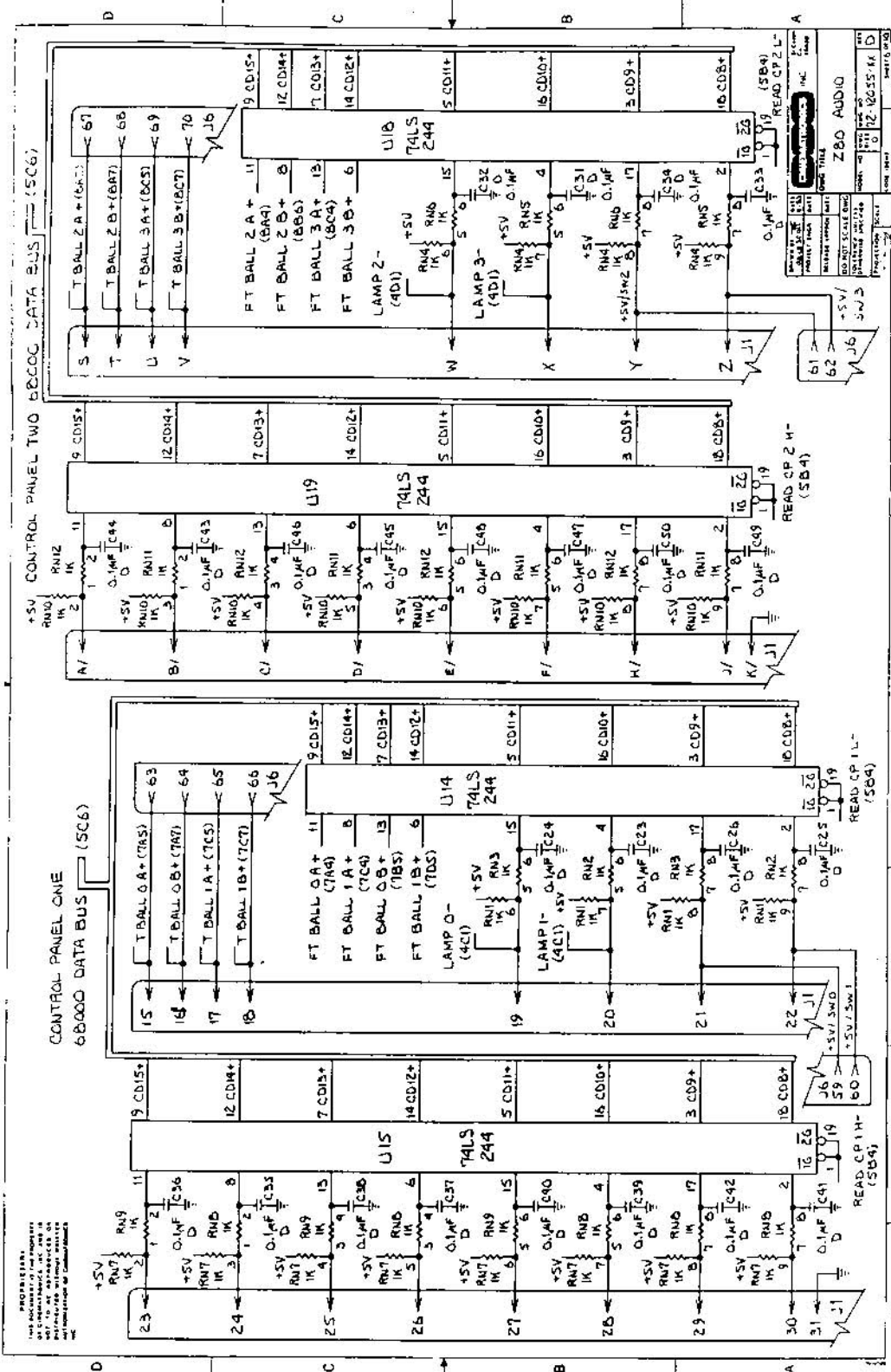
NOTES UNLESS OTHERWISE SPECIFIED





PARTS LIST		QTY		DESCRIPTION	
U48	LS14	1	1	LS14	
U49	LS02	1	1	LS02	
U75	LS244	2	2	LS244	
U81	74LS04	2	2	74LS04	
U80	74LS393	1	1	74LS393	
U69	74LS244	1	1	74LS244	
U68	74LS244	1	1	74LS244	
Q2	2N5210	1	1	2N5210	
Q3	2N4209	1	1	2N4209	
Q4	2N2369A	1	1	2N2369A	
Y1	14.31815 MHz	1	1	14.31815 MHz	
C133	680PF	1	1	680PF	
R130	4.7K	1	1	4.7K	
R138	1K	1	1	1K	
R142	18K	1	1	18K	
R141	3K	1	1	3K	
R139	1K	1	1	1K	
R143	330	1	1	330	
R144	330	1	1	330	
R133	68	1	1	68	
R134	300	1	1	300	
R135	1.1K	1	1	1.1K	
R113	470	1	1	470	
R114	470	1	1	470	
R112	470	1	1	470	

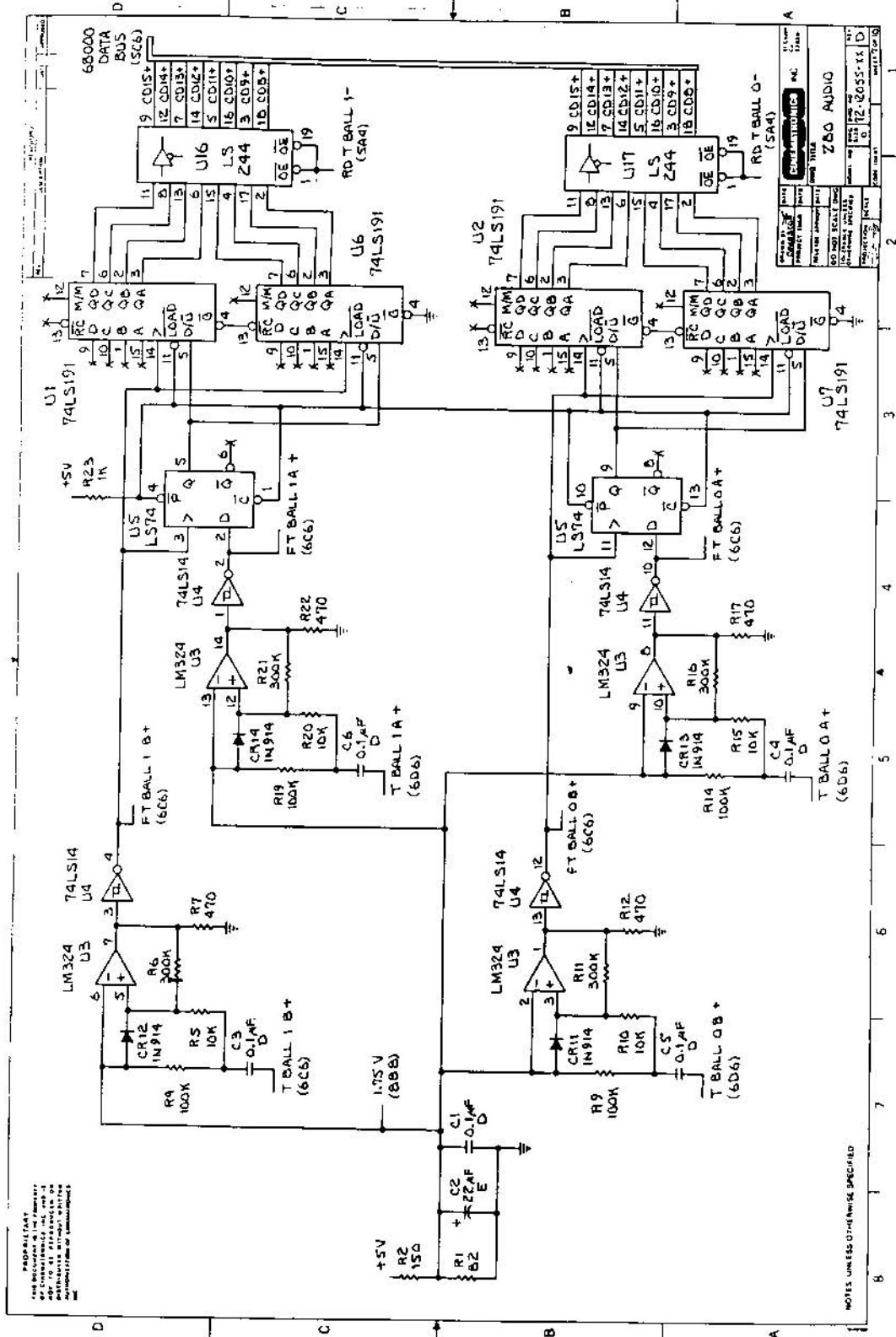
Z80 EXPANSION		QTY		DESCRIPTION	
DIR RD-1	19	1	1	DIR RD-1	
DIR RD-2	20	1	1	DIR RD-2	
DIR RD-3	21	1	1	DIR RD-3	
DIR RD-4	22	1	1	DIR RD-4	
DIR RD-5	23	1	1	DIR RD-5	
DIR RD-6	24	1	1	DIR RD-6	
DIR RD-7	25	1	1	DIR RD-7	
DIR RD-8	26	1	1	DIR RD-8	
DIR RD-9	27	1	1	DIR RD-9	
DIR RD-10	28	1	1	DIR RD-10	
DIR RD-11	29	1	1	DIR RD-11	
DIR RD-12	30	1	1	DIR RD-12	
DIR RD-13	31	1	1	DIR RD-13	
DIR RD-14	32	1	1	DIR RD-14	
DIR RD-15	33	1	1	DIR RD-15	
DIR RD-16	34	1	1	DIR RD-16	
DIR RD-17	35	1	1	DIR RD-17	
DIR RD-18	36	1	1	DIR RD-18	
DIR RD-19	37	1	1	DIR RD-19	
DIR RD-20	38	1	1	DIR RD-20	
DIR RD-21	39	1	1	DIR RD-21	
DIR RD-22	40	1	1	DIR RD-22	
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DIR RD-40				DIR RD-40	



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DESIGN NO.	100-355
REVISION	1.0
DATE	1984.02.10
PROJECT	CONTROL PANEL DATA BUS (SC66)
DESIGNED BY	W.H. PARK
CHECKED BY	J.S. LEE
DATE	1984.02.10
APP'D BY	W.H. PARK
DATE	1984.02.10
FILE NO.	100-355-1A
WORK SHEET	1 OF 1

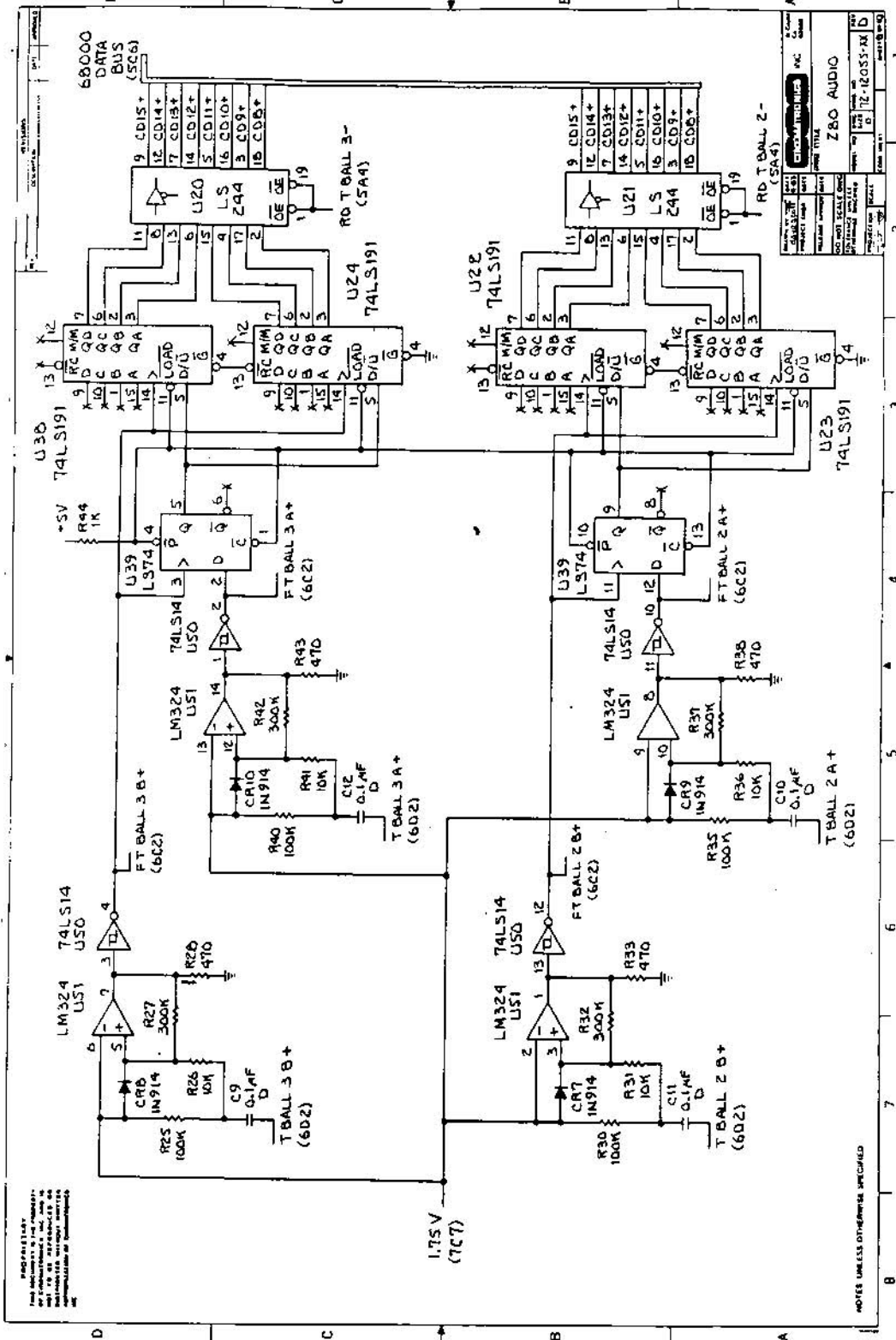
BOARD TITLE: CONTROL PANEL DATA BUS (SC66)
 BOARD TYPE: 2300 (SBA0)
 PART NO: 100-355-1A
 REV: 1.0
 DATE: 1984.02.10



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DATE	REV	BY	CHKD
12-20-85	1	JL	ML
PROJECT NAME: Z80 AUDIO			
DO NOT SCALE DRAWING			
DRAWN BY: JL			
CHECKED BY: ML			
APPROVED BY: ML			
SCALE: 1:1			
SHEET NO. 1 OF 1			



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 WORK
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 DATE 08-14-2001 BY 60320
 (U)

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NO.	REV.	DATE	BY	CHK.	APP.
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68000 DATA BUS (5CG6)

RD T BALL 3- (5A4)

RD T BALL 2- (5A4)

Z80 AUDIO

1.75V (7C7)

+5V R44 1K

FT BALL 3B+ (6C2)

T BALL 3A+ (6D2)

FT BALL 2A+ (6C2)

T BALL 2A+ (6D2)

FT BALL 3B+ (6C2)

T BALL 3A+ (6D2)

FT BALL 2A+ (6C2)

T BALL 2A+ (6D2)

FT BALL 3B+ (6C2)

T BALL 3A+ (6D2)

FT BALL 2A+ (6C2)

T BALL 2A+ (6D2)

FT BALL 3B+ (6C2)

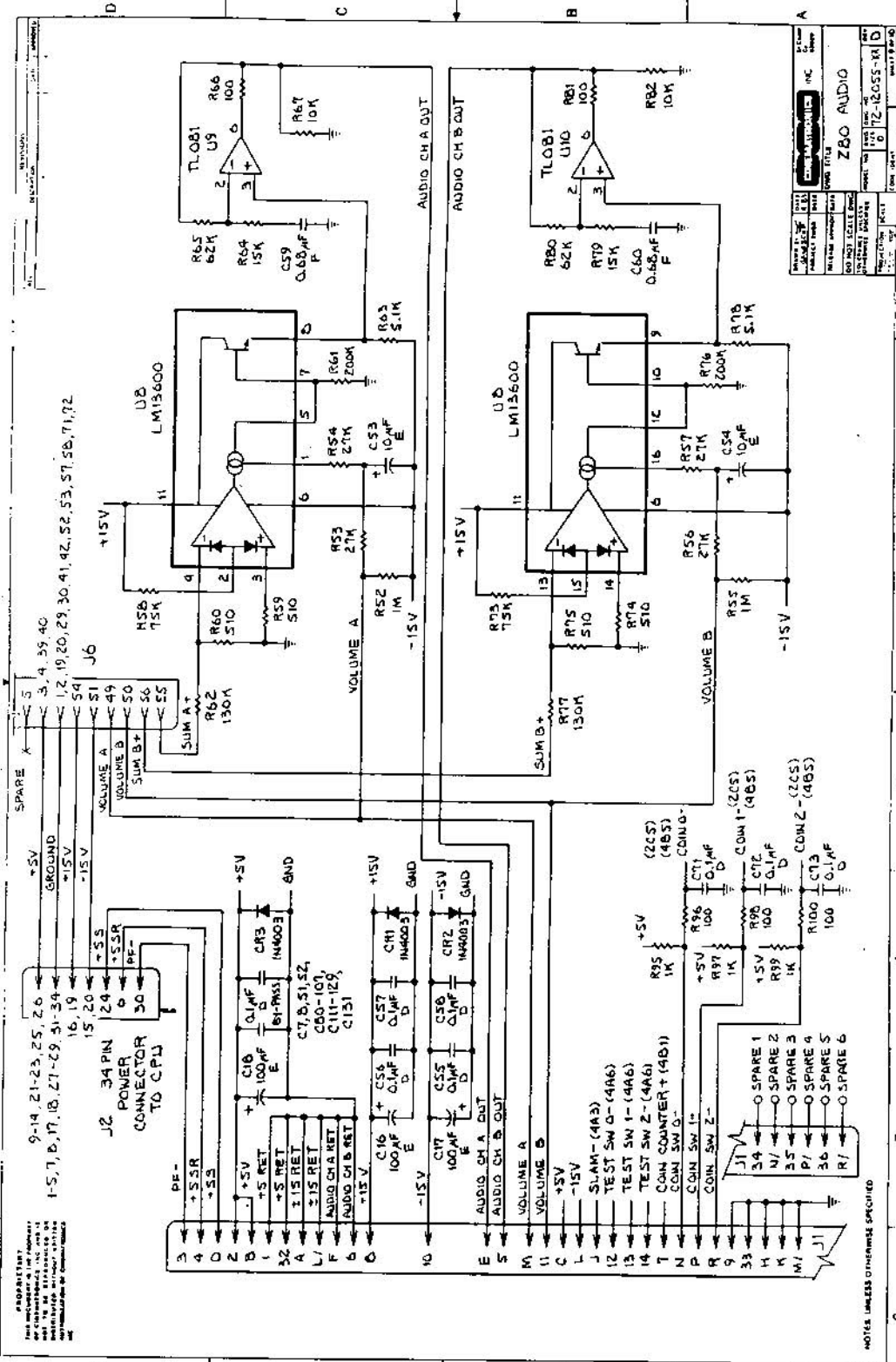
T BALL 3A+ (6D2)

FT BALL 2A+ (6C2)

T BALL 2A+ (6D2)

FT BALL 3B+ (6C2)

T BALL 3A+ (6D2)



9-14, 21-23, 25, 26 → +5V
 3, 4, 35, 40 → GROUND
 1-5, 7, 8, 17, 18, 27-29, 31-34 → +5V
 12, 19, 20, 29, 30, 41, 42, 52, 53, 57, 58, 71, 72 → +5V
 15, 20 → -15V
 15, 20 → -5V
 24 → +5V
 25 → +5V
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REV	DATE	BY	DESCRIPTION
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Z80 AUDIO
 REV 1
 DATE 1/15/80
 BY J. J. BROWN
 CHECKED BY J. J. BROWN
 APPROVED BY J. J. BROWN
 PART NO. Z80-AUDIO-1
 QTY. 100
 UNIT PRICE \$1.50
 TOTAL \$150.00
 DRAWING NO. Z80-AUDIO-1
 SHEET 1 OF 1
 PROJECT NO. 72-12055-1A
 DRAWING NO. Z80-AUDIO-1
 SHEET 1 OF 1

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IC REFERENCE	+5V	GND
U33	24	5
U13, U14, U15, U16, U17, U18, U19, U20, U21, U27, U28, U29, U30, U44, U45, U46, U47, U56, U57, U63, U64, U65, U66, U67, U68, U69, U70, U72, U73, U74, U75	20	10
U50, U59	10	9
U1, U2, U5, U7, U22, U23, U24, U30, U32, U33, U54, U55, U77, U10, U79 U4, U5, U11, U12, U26, U34, U35, U36, U37, U39, U40, U41, U42, U43, U47, U48, U49, U50, U60, U61, U62, U76, U80, U81	16	0
U71	11	29
U3, U51	4	11
U31, U32	5	6
U7, U47, U70	1	NAME

IC REFERENCE	+15V	-15V
U8	11	6
U9, U10	7	4

LAST REFERENCE DESIGNATORS USED:
U81, R145, C13, D19, Q6, R112, J6
REFERENCE DESIGNATORS DELETED:
R3, D, B, 13, 15, 24, 29, 39, 39, 60-72,
R86-94, 125, 126, 132, 136,
C13-15, 19-22, 25-30, 61-70, 75,
C79, 108, 109, 132,
U25

IC REFERENCE	ENABLING PINS	OUTPUT PINS ENABLED
U63	1, 19	3, 5, 14, 16, 18
U73	1, 19	5, 7, 9, 12, 14

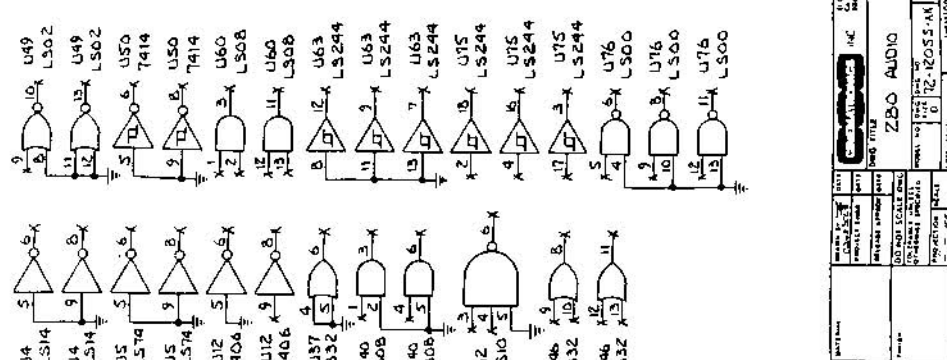
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J1

PIN	FUNCTION	LOCATION
1	+5 RETURN	(9C8)
2	PR	(9C9)
3	PR	(9D3)
4	+5SR	(9D3)
5	AUDIO CH B OUT	(9D8)
6	AUDIO CH B RET	(9D8)
7	CON COUNTER	(9D8)
8	GROUND	(9E5)
9	GROUND	(9E8)
10	VOLUME	(9E8)
11	TEST SW 0	(9E8)
12	TEST SW 1	(9E8)
13	TEST SW 2	(9E8)
14	T BALL 0 +	(9E8)
15	T BALL 0 -	(9E8)
16	T BALL 1 +	(9E8)
17	T BALL 1 -	(9E8)
18	LAMP 0 - SWITCH INPUT	(6C6)
19	LAMP 0 + SWITCH INPUT	(6C6)
20	LAMP 1 - SWITCH INPUT	(6C6)
21	LAMP 1 + SWITCH INPUT	(6C6)
22	+5V/SW1	(6A6)
23	+5V/SW1	(6A6)
24	SWITCH INPUTS FOR PANEL ONE	(6C8)
25	GROUND	(6A8)
26	GROUND	(6A8)
27	SEL ROM 0	(9C5)
28	SEL ROM 1	(9C5)
29	SPARE 1	(9A7)
30	SPARE 2	(9A7)
31	SPARE 3	(9A7)
32	-15 RETURN	(9C8)
33	+5V	(9E8)
34	+5V	(9E8)
35	AUDIO CH A OUT	(9D8)
36	AUDIO CH A RET	(9D8)
37	SLAM	(9A8)
38	GROUND	(9A8)
39	GROUND	(9A8)
40	VOLUME A	(9A8)
41	CON SW 0	(9A8)
42	CON SW 1	(9A8)
43	T BALL 2 +	(6D3)
44	T BALL 2 -	(6D3)
45	T BALL 3 +	(6D3)
46	T BALL 3 -	(6D3)
47	LAMP 2 - SWITCH INPUT	(6B3)
48	LAMP 2 + SWITCH INPUT	(6B3)
49	+5V/SW 2	(6B3)
50	+5V/SW 2	(6B3)
51	+5V/SW 3	(6A4)
52	+5V/SW 3	(6A4)
53	SWITCH INPUTS FOR CONTROL PANEL TWO	(6C4)
54	GROUND	(6A4)
55	GROUND	(6A4)
56	-15 RETURN	(6C4)
57	GROUND	(6A4)
58	SPARE 4	(9A7)
59	SPARE 5	(9A7)
60	SPARE 6	(9A7)

J6

PIN	FUNCTION	LOCATION
1	GROUND	(9D5)
2	GROUND	(9D5)
3	+5V	(9D5)
4	SPARE	(9D3)
5	BA1Z +	(9D3)
6	BA1Z +	(9D3)
7	BA0 +	(9D3)
8	BA0 +	(9D3)
9	BA0 +	(9D3)
10	BA0 +	(9D3)
11	BA0 +	(9D3)
12	BA5 +	(9D3)
13	BA5 +	(9D3)
14	BA3 +	(9D3)
15	BA3 +	(9D3)
16	BA1 +	(9D3)
17	BA1 +	(9D3)
18	BA0 +	(9D3)
19	GROUND	(9D5)
20	GROUND	(9D5)
21	BD1 +	(9D3)
22	BD1 +	(9D3)
23	BD3 +	(9D3)
24	BD3 +	(9D3)
25	BD2 +	(9D3)
26	BD2 +	(9D3)
27	BD1 +	(9D3)
28	BD1 +	(9D3)
29	GROUND	(9D5)
30	GROUND	(9D5)
31	SEL ROM 0	(9D3)
32	SEL ROM 1	(9D3)
33	SEL ROM 2	(9D3)
34	SEL ROM 3	(9D3)
35	SPARE 5	(9A3)
36	SPARE 6	(9A3)
37	BW1 -	(9A3)
38	NPL -	(9A3)
39	+5V	(9D5)
40	+5V	(9D5)
41	GROUND	(9D5)
42	GROUND	(9D5)
43	G10 +	(9D5)
44	G11 +	(9D5)
45	C1C 1 -	(2D1)
46	C1C 1 +	(2D1)
47	EXT AUDIO 0 +	(9A1)
48	EXT AUDIO 1 +	(9A1)
49	VOLUME A	(9D5)
50	VOLUME B	(9D5)
51	-15V	(9D5)
52	GROUND	(9D5)
53	+15V	(9D5)
54	SUM A +	(9D5)
55	SUM B +	(9D5)
56	GROUND	(9D5)
57	GROUND	(9D5)
58	+2V/SW 4	(6A7)
59	+2V/SW 4	(6A7)
60	+5V/SW 2	(6A3)
61	+5V/SW 2	(6A3)
62	T BALL 0 A +	(6D3)
63	T BALL 0 A -	(6D3)
64	T BALL 1 A +	(6D3)
65	T BALL 1 A -	(6D3)
66	T BALL 2 A +	(6D3)
67	T BALL 2 A -	(6D3)
68	T BALL 3 A +	(6D3)
69	T BALL 3 A -	(6D3)
70	GROUND	(9D5)
71	GROUND	(9D5)
72	GROUND	(9D5)



UNIT TITLE
ZBO AUDIO

FORM NO. 10-112-12055-AN D
DATE 1-15-60

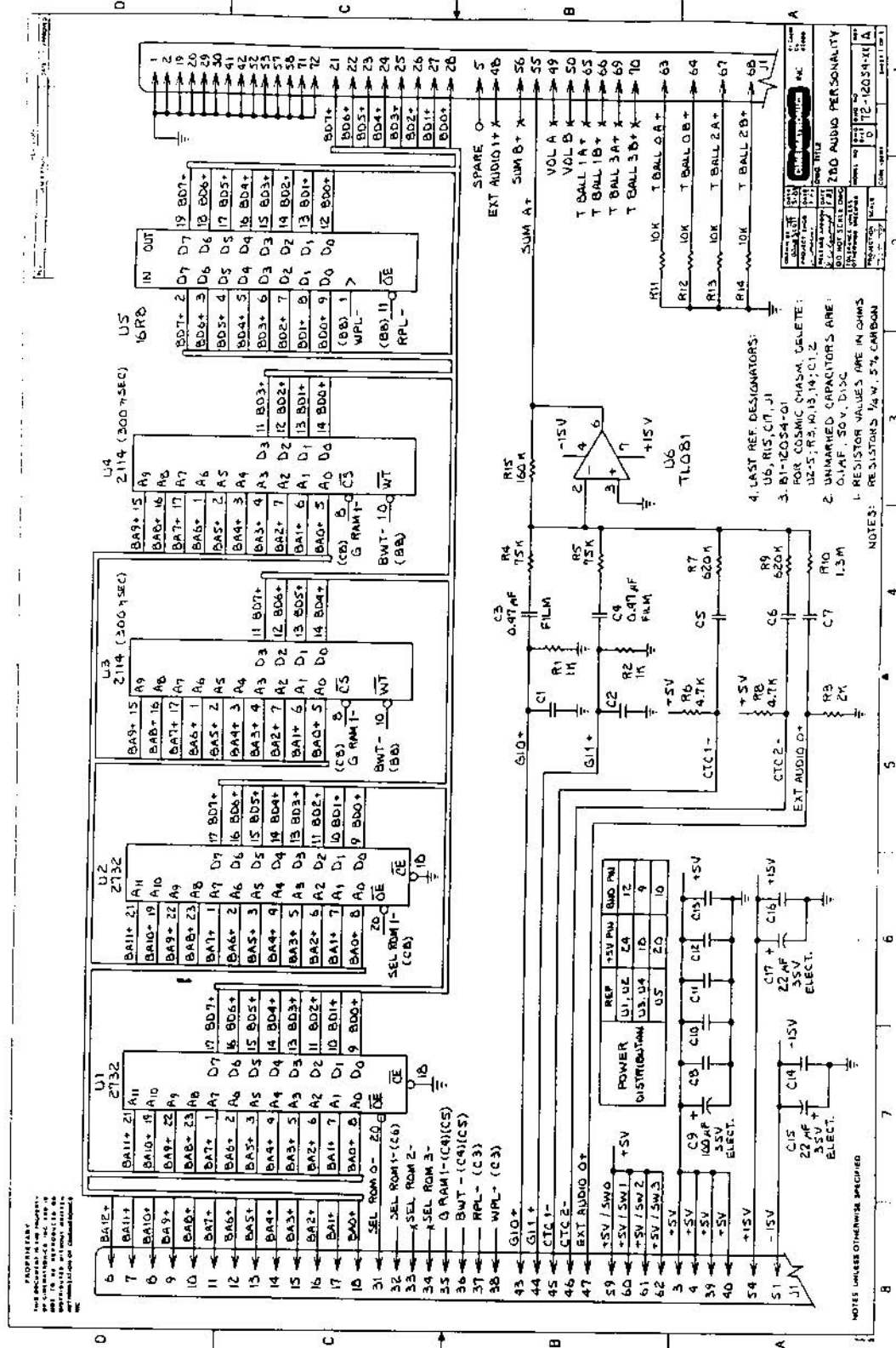
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CONTROL: [] UNCLASSIFIED [] CONFIDENTIAL [] SECRET

CLASSIFICATION: UNCLASSIFIED

EXEMPTION CODE:

FORM NO. 10-112-12055-AN D
DATE 1-15-60



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Pin	Symbol	Function
5	SPARE	0
6	BA12+	
7	BA11+	
8	BA10+	
9	BA9+	
10	BA8+	
11	BA7+	
12	BA6+	
13	BA5+	
14	BA4+	
15	BA3+	
16	BA2+	
17	BA1+	
18	BA0+	
19	BD7+	
20	BD6+	
21	BD5+	
22	BD4+	
23	BD3+	
24	BD2+	
25	BD1+	
26	BD0+	
27	BD7+	
28	BD6+	
29	BD5+	
30	BD4+	
31	BD3+	
32	BD2+	
33	BD1+	
34	BD0+	
35	SEL ROM 0 - 20	OE
36	SEL ROM 1 - 21	OE
37	SEL ROM 2 - 22	OE
38	SEL ROM 3 - 23	OE
39	SEL ROM 4 - 24	OE
40	SEL ROM 5 - 25	OE
41	SEL ROM 6 - 26	OE
42	SEL ROM 7 - 27	OE
43	SEL ROM 8 - 28	OE
44	SEL ROM 9 - 29	OE
45	SEL ROM 10 - 30	OE
46	SEL ROM 11 - 31	OE
47	SEL ROM 12 - 32	OE
48	SEL ROM 13 - 33	OE
49	SEL ROM 14 - 34	OE
50	SEL ROM 15 - 35	OE
51	SEL ROM 16 - 36	OE
52	SEL ROM 17 - 37	OE
53	SEL ROM 18 - 38	OE
54	SEL ROM 19 - 39	OE
55	SEL ROM 20 - 40	OE
56	SEL ROM 21 - 41	OE
57	SEL ROM 22 - 42	OE
58	SEL ROM 23 - 43	OE
59	SEL ROM 24 - 44	OE
60	SEL ROM 25 - 45	OE
61	SEL ROM 26 - 46	OE
62	SEL ROM 27 - 47	OE
63	SEL ROM 28 - 48	OE
64	SEL ROM 29 - 49	OE
65	SEL ROM 30 - 50	OE
66	SEL ROM 31 - 51	OE
67	SEL ROM 32 - 52	OE
68	SEL ROM 33 - 53	OE
69	SEL ROM 34 - 54	OE
70	SEL ROM 35 - 55	OE
71	SEL ROM 36 - 56	OE
72	SEL ROM 37 - 57	OE
73	SEL ROM 38 - 58	OE
74	SEL ROM 39 - 59	OE
75	SEL ROM 40 - 60	OE
76	SEL ROM 41 - 61	OE
77	SEL ROM 42 - 62	OE
78	SEL ROM 43 - 63	OE
79	SEL ROM 44 - 64	OE
80	SEL ROM 45 - 65	OE
81	SEL ROM 46 - 66	OE
82	SEL ROM 47 - 67	OE
83	SEL ROM 48 - 68	OE
84	SEL ROM 49 - 69	OE
85	SEL ROM 50 - 70	OE
86	SEL ROM 51 - 71	OE
87	SEL ROM 52 - 72	OE
88	SEL ROM 53 - 73	OE
89	SEL ROM 54 - 74	OE
90	SEL ROM 55 - 75	OE
91	SEL ROM 56 - 76	OE
92	SEL ROM 57 - 77	OE
93	SEL ROM 58 - 78	OE
94	SEL ROM 59 - 79	OE
95	SEL ROM 60 - 80	OE
96	SEL ROM 61 - 81	OE
97	SEL ROM 62 - 82	OE
98	SEL ROM 63 - 83	OE
99	SEL ROM 64 - 84	OE
100	SEL ROM 65 - 85	OE
101	SEL ROM 66 - 86	OE
102	SEL ROM 67 - 87	OE
103	SEL ROM 68 - 88	OE
104	SEL ROM 69 - 89	OE
105	SEL ROM 70 - 90	OE
106	SEL ROM 71 - 91	OE
107	SEL ROM 72 - 92	OE
108	SEL ROM 73 - 93	OE
109	SEL ROM 74 - 94	OE
110	SEL ROM 75 - 95	OE
111	SEL ROM 76 - 96	OE
112	SEL ROM 77 - 97	OE
113	SEL ROM 78 - 98	OE
114	SEL ROM 79 - 99	OE
115	SEL ROM 80 - 100	OE

NOTES:
1. RESISTOR VALUES ARE IN OHMS
2. UNMARKED CAPACITORS ARE:
0.1 uF, 50V, D35C
3. B1-12054-01
FOR COSMIC CHASSIS CARTE:
12-5, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100
4. LAST REF DESIGNATORS:
U6, R15, C17, J1
3. B1-12054-01

U1 2732
U2 2732
U3 2114 (20075SEC)
U4 2114 (30075SEC)
U5 16RB
U6 TL081

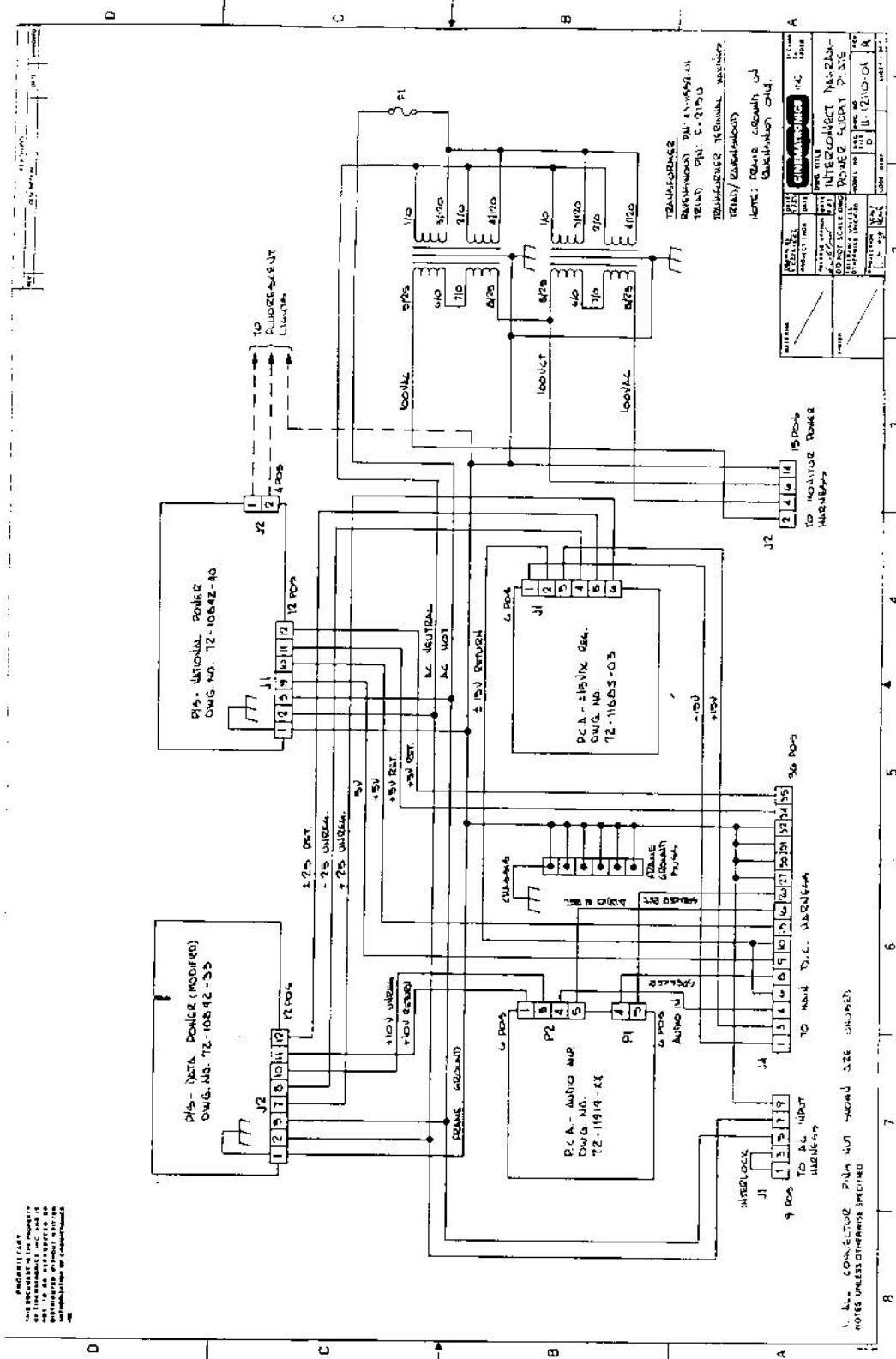
POWER DISTRIBUTION
+5V / SW1
+5V / SW2
+5V / SW3
+5V
+5V
+5V
+15V
-15V

EXT AUDIO IN X
SUM A
SUM B X
VOL A X
VOL B X
T BALL 1 A X
T BALL 1 B X
T BALL 3 A X
T BALL 3 B X
T BALL 2 A X
T BALL 2 B X

REVISIONS
REV 1
REV 2
REV 3
REV 4
REV 5
REV 6
REV 7
REV 8
REV 9
REV 10
REV 11
REV 12

D C B A
1 2 3 4 5 6 7 8
A B C D

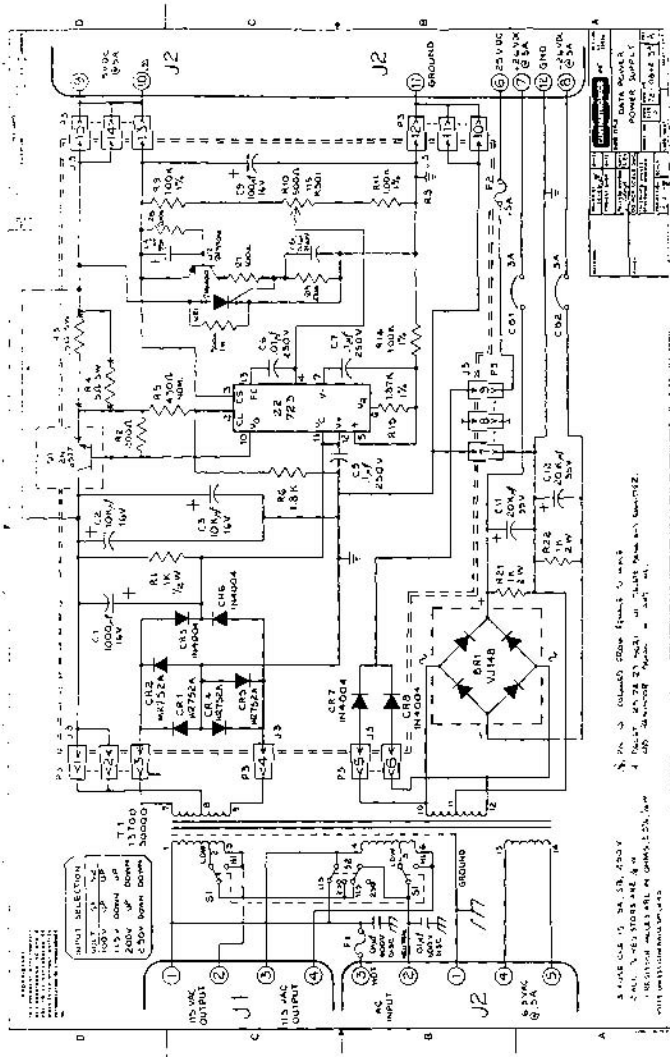
PROPRIETARY
 INFORMATION
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PROJECT NO.		DATE	
DRAWING NO.		REV.	
SHEET NO.		TOTAL SHEETS	
PROJECT TITLE		PROJECT NO.	
DRAWING TITLE		DRAWING NO.	
DESIGNED BY		CHECKED BY	
DRAWN BY		DATE	

TRANSFORMER
 SUPPLY FROM 4170V/110V
 TURNS: 5-270V
 TRANSFORMER TERMINAL MARKINGS
 TURNS/ VOLTAGE
 HOME: 150V 270V 4170V

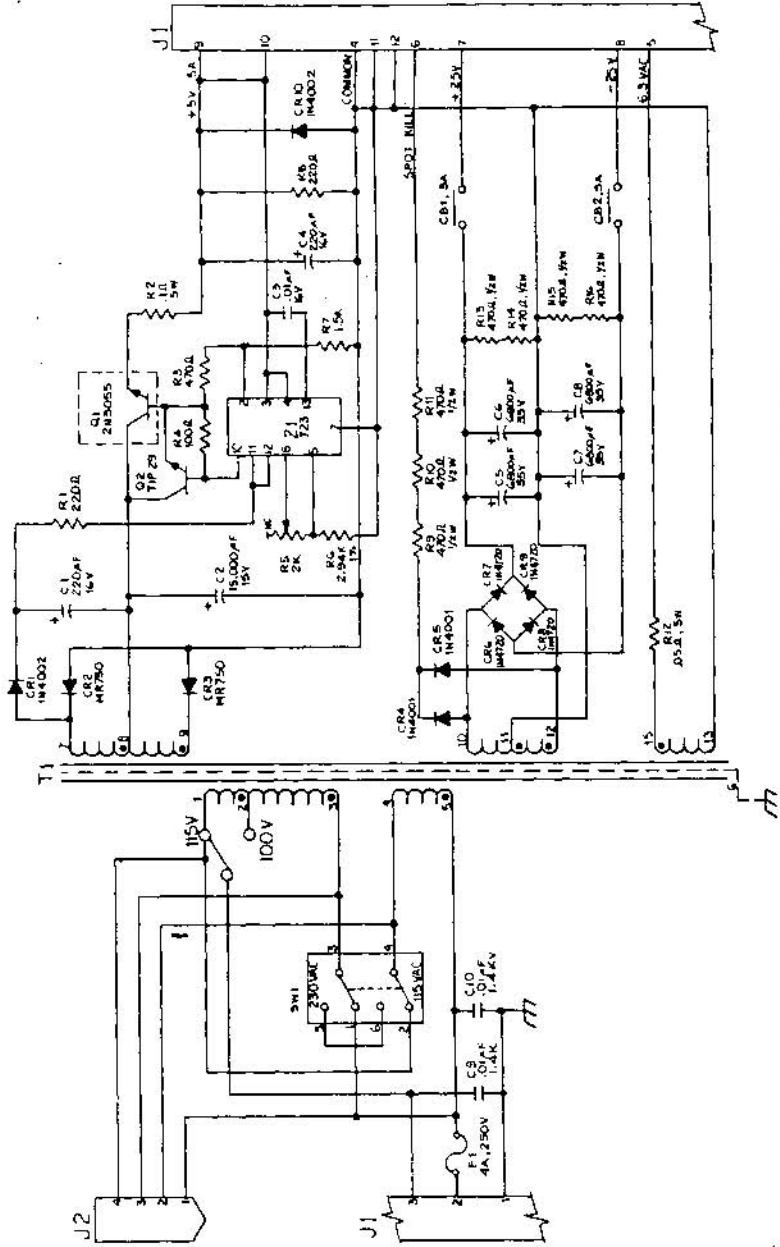
U.S. CONNECTOR PINN NOT SHOWN ARE UNUSED
 NOTES UNLESS OTHERWISE SPECIFIED



1. USE 115V 20A 50/60HZ
 2. ALL RESISTORS ARE 1/4W
 3. RESISTOR TOLERANCE IS 5% UNLESS OTHERWISE SPECIFIED
 4. CAPACITOR TOLERANCE IS 5% UNLESS OTHERWISE SPECIFIED
 5. CAPACITOR VOLTAGE RATING IS 20% ABOVE OPERATING VOLTAGE

NO.	DESCRIPTION	QTY.	REMARKS
1	115V AC OUTPUT (J1)	1	
2	AC INPUT (J2)	1	
3	5.25V DC OUTPUT (J3)	1	
4	115V DC OUTPUT (J4)	1	

REVISIONS		DATE	APPROVED
1	REWORK TYPE	4 DEC 60	BA
A. PRODUCTION RELEASE			
2	ADD 50-10-566 E.C. 0026-7	23 JAN 61	BA
DWG NO. PRDM 12A002B-00			

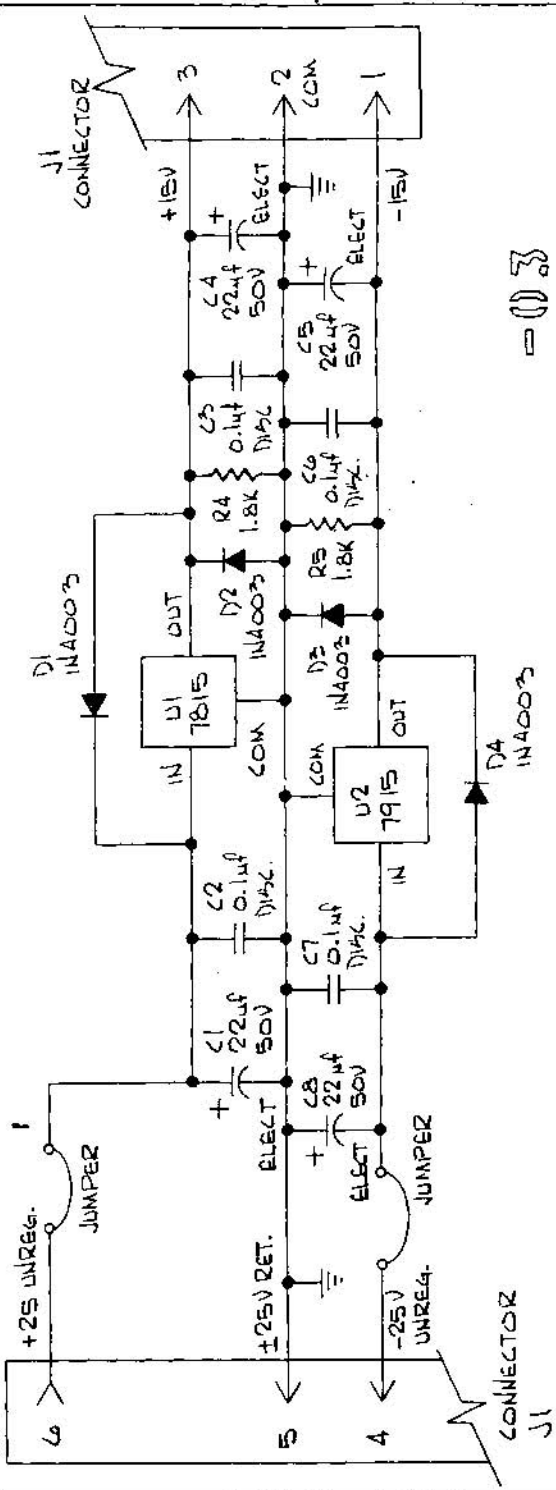


QTY. PART OR IDENT.		PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION	
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS TO DECIMALS ANGLES IN DEGREES					
CONTRACT NO.					
APPROVALS		DATE		REV	
DESIGNED BY		DRAWN BY		CHECKED BY	
NATIONAL POWER TECHNOLOGY		POWER SUPPLY		72-10242-90	
DWG NO. PRDM 12A002B-00		SHEET NO. 1 OF 1		REV B	
APP. 100%		USED ON		DATE	
APPROVED		SCALE		SHEET 1 OF 1	

4-204 (REV. 7-55) (2)

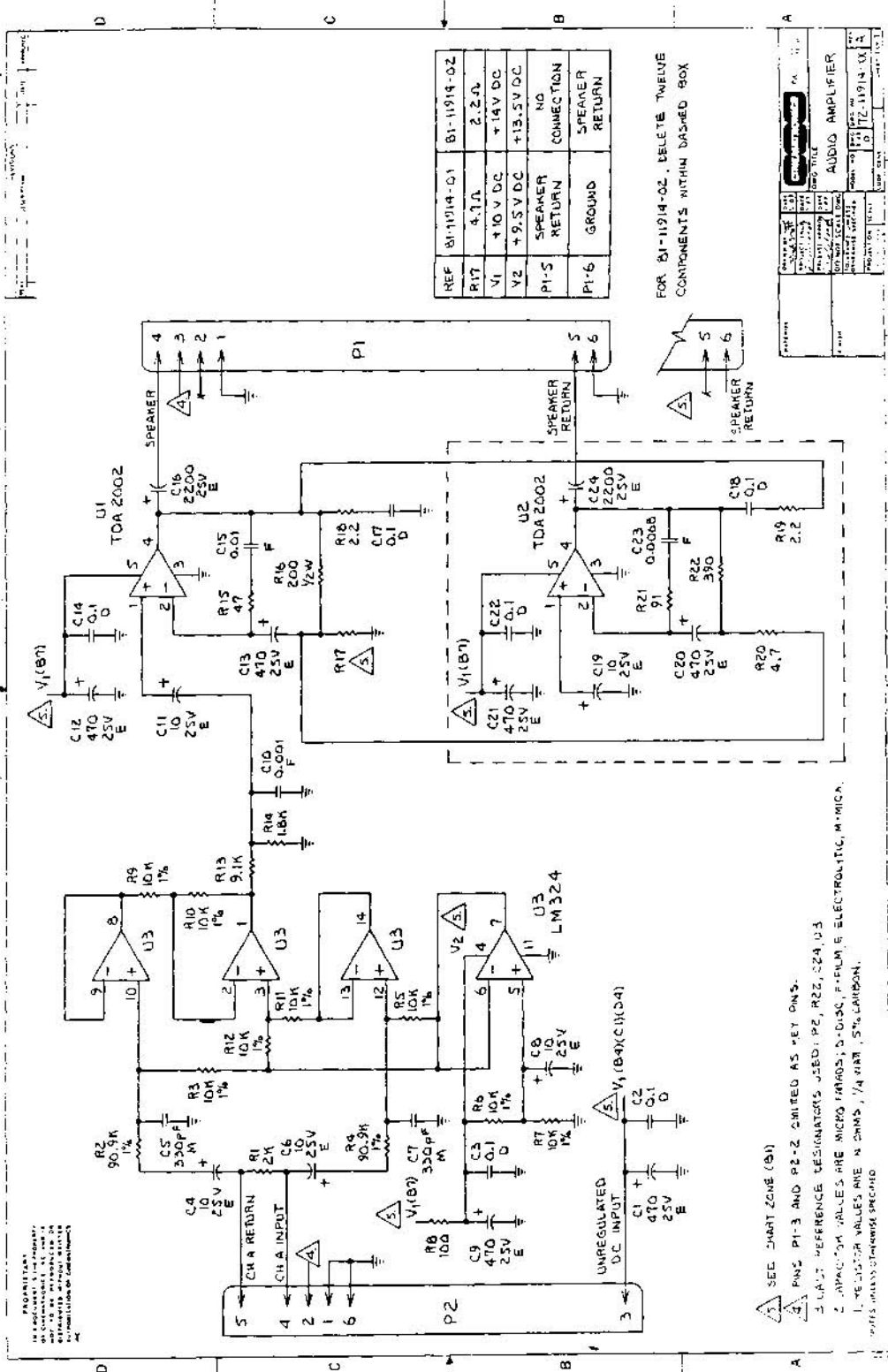
REV	DESCRIPTION	DATE	APPROVED

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 AUTHORIZATION OF CINEMATRONICS
 INC.



UNUSED DES:
 R1, R2, R3
 LAY1 DES:
 C8, D4, R5
 2. R4 AND R5 VALUES ARE IN OHMS.
 1. R4 AND R5 ARE 1/4 WATTS, 5% CARBON.
 NOTES:

MATERIAL:		DATE	DATE	DATE	DATE
FINISH: BREAK ALL SHARP EDGES AND DEBURR ALL HOLES.		5-28-72	5-28-72	5-28-72	5-28-72
DO NOT SCALE DWG TOLERANCE UNLESS OTHERWISE SPECIFIED		PROJECT ENGR.	DATE	DATE	DATE
PROJECTION: SCALE: NONE		5-28-72	5-28-72	5-28-72	5-28-72
CINEMATRONICS INC.		DWG TITLE			
E1 C1010 C1 92020		REGULATOR +15 -15 VOLTS			
MODEL NO. DWG NO.		REV		REV	
72-11685-03		B		A	
CODE IDENT.		SHEET 1 OF 1			



- 1. SEE CHART ZONE (B1)
- 2. PINS P1-3 AND P2-2 OMITTED AS KEY PINS.
- 3. LAYOUT REFERENCE DESIGNATORS USED: P2, R22, C24, U3
- 4. APPROXIMATE VALUES ARE MICROFARADS; 5-DIGIT FILM ELECTRONIC, M.M.I.C.A.
- 5. RESISTOR VALUES ARE IN OHMS, 1/4 WATT, 5% TOLERANCE CARBON FILM.

REV.	DATE	BY	CHKD.	DESCRIPTION
1				ISSUED FOR PRODUCTION
2				REVISION
3				REVISION
4				REVISION
5				REVISION
6				REVISION
7				REVISION
8				REVISION
9				REVISION
10				REVISION
11				REVISION
12				REVISION
13				REVISION
14				REVISION
15				REVISION
16				REVISION
17				REVISION
18				REVISION
19				REVISION
20				REVISION
21				REVISION
22				REVISION
23				REVISION
24				REVISION
25				REVISION
26				REVISION
27				REVISION
28				REVISION
29				REVISION
30				REVISION

PRODUCTION PART NO. 81-11914-01

DATE: 11/11/71

BY: [Signature]

CHKD: [Signature]

DESCRIPTION: AUDIO AMPLIFIER

COSMIC CHASM ONBOARD TEST

1. Push reset switch next to DIP switch on processor board
2. Push test button on panel with volume control and coin counter
3. Color test pattern should now appear on screen
4. Push test button again
5. Crosshatch test pattern should appear on screen
6. Push test button again
7. You should now be in control panel/audio test mode.

NOTE: Audio will be heard only if attract mode audio is turned on (processor DIP switch, position 6)

A spaceship and multicolored test pattern should appear. Rotating shaft encoder should rotate ship
Pushing thrust button(s) should cause ship to move slowly with thrust sound.
Pushing fire button(s) should cause ship to fire with fire sound.
Pushing shield button(s) should cause shield to appear with shield sound.
Pushing one or two player start buttons should cause "ONE PLAYER" or "TWO PLAYER" to appear at bottom of screen.

8. Push test button again.
9. You should now be in game configuration mode.

Game setup information and a multicolored test pattern should be on the screen.
Changing the setting of the DIP switch on the processor board should change the corresponding information on the display.

10. Push the reset button on the processor board to exit test mode and enter changes in the game setup.

NOTE: Turning position 8 of the processor DIP switch "on" has the same effect as pushing the test button.

4/6/83