Regulator/Audio II PCB Schematic (035435-02 B)

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

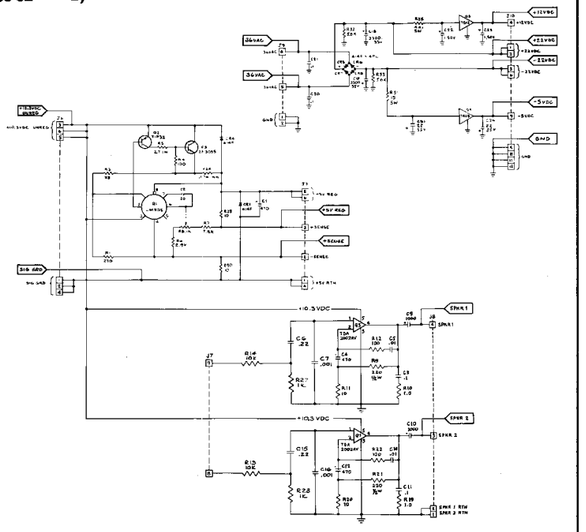
The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and −SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

Regulator Adjustment

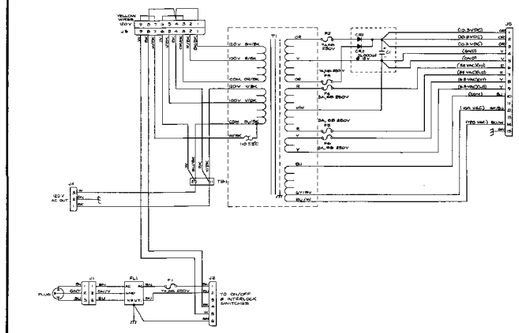
1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio PCB and plus lead to +5 V test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

Audio Circuit

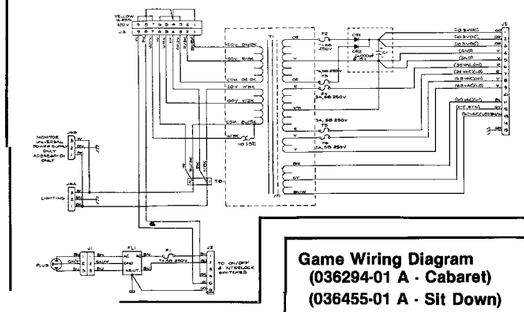
The audio circuit contains two independent audio amplifiers. Each consists of a TDA2002AV amplifier with a gain of ten.



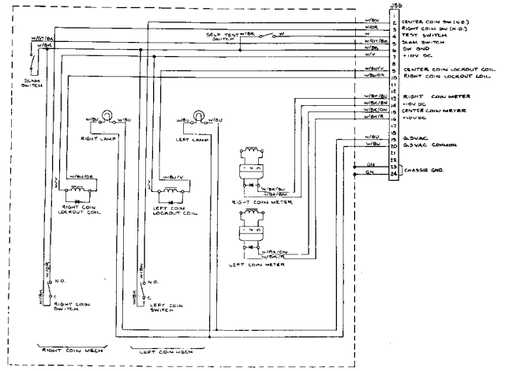
Power Supply Wiring Diagram (036097-01 B Cabaret)

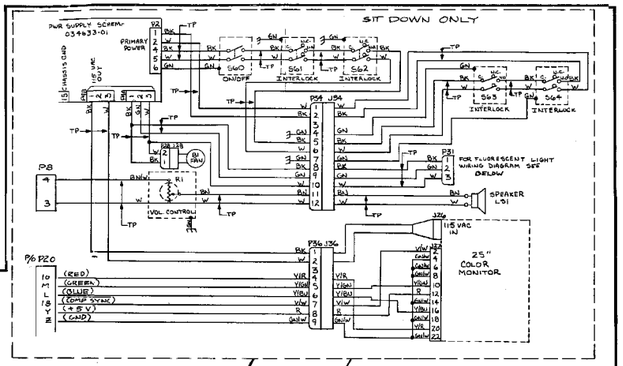


Power Supply Wiring Diagram (034633-01 B Sit Down)

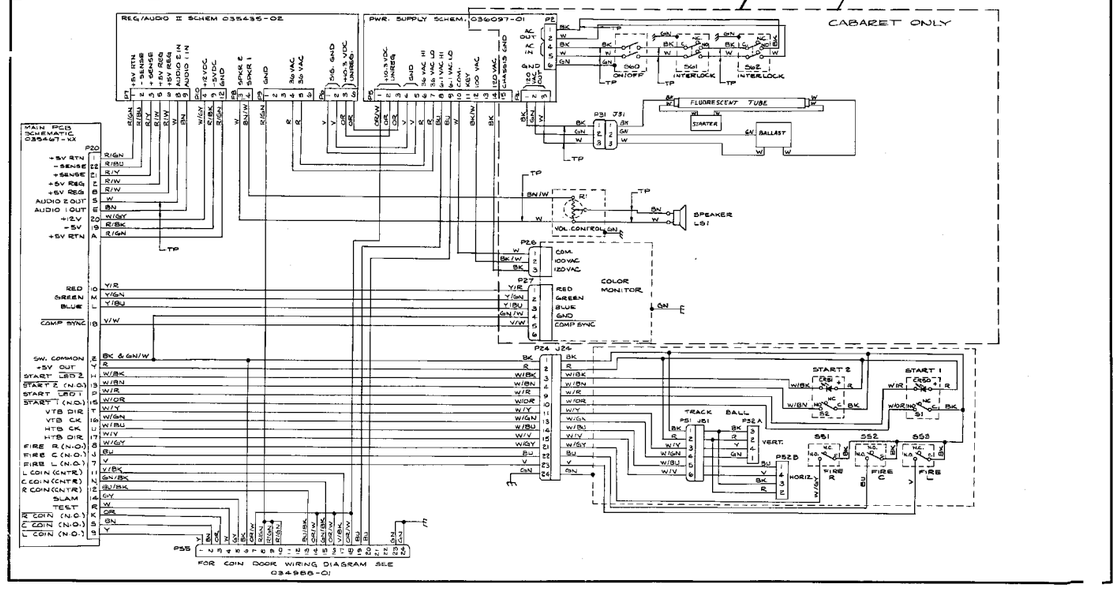


Coin Door Schematic (034988-01 A)





Game Wiring Diagram (036294-01 A - Cabaret) (036455-01 A - Sit Down)



Drawing Package Supplement

to

MISSILE COMMAND™

Operation, Maintenance, and Service Manual

Contents of this Drawing Package

ATARI®

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Sheet 1, Side A
DP-158-01 1st printing

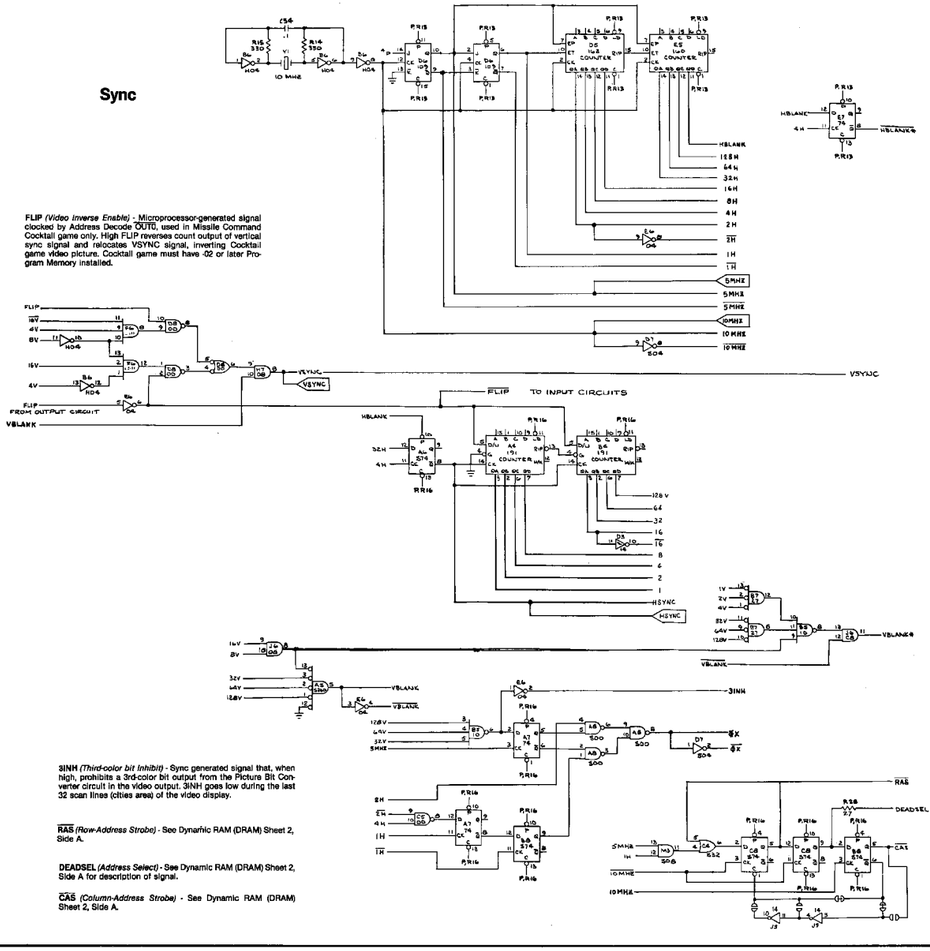
DIAGNOSTIC TESTS

Instruction	Use of Test
1. Set self-test switch to **on** position. Note: entering self-test will set the HIGH SCORE TODAY display to 7500.	
2. Press alpha base fire button and slam switch simultaneously. Release slam switch first.	A convergence pattern appears on the monitor screen. The background can be many possible colors. If you are going to converge the monitor, black is the color you want. To change background color, press either START button. **Do not attempt any convergence adjustments unless you are a qualified color TV technician!**
3. Press omega base fire button and slam switch simultaneously. Release slam switch first.	Vertical color bars appear on the screen, to permit color hue and brightness adjustments. Pressing either start button changes the color of the right and left vertical bars. **Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!**
4. Press delta base fire button and slam switch simultaneously.	White screen appears, and tiny black dots trace all the raster lines from top to bottom (takes about 47 seconds). After this, a blue **RAM OK** message appears on the screen, and the + will reappear. If the message **BAD RAM** appears and some or all of the digits 1 thru 8, refer to the following to determine the failing RAM chips.

Test no. 4 display	*Bad chip location*
BAD RAM 8	P4
BAD RAM 7	N4
BAD RAM 6	M4
BAD RAM 5	L4
BAD RAM 4	K4
BAD RAM 3	J4
BAD RAM 2	H4
BAD RAM 1	F4

5. Set self-test switch to **off** position.	Check attract mode display and readjust brightness if necessary.

Sync



FLIP *(Video Inverse Enable)* - Microprocessor-generated signal clocked by Address Decode OUT0, used in Missile Command Cocktail game only. High FLIP reverses count output of vertical sync signal and relocates VSYNC signal, inverting Cocktail game video picture. Cocktail game must have -02 or later Program Memory installed.

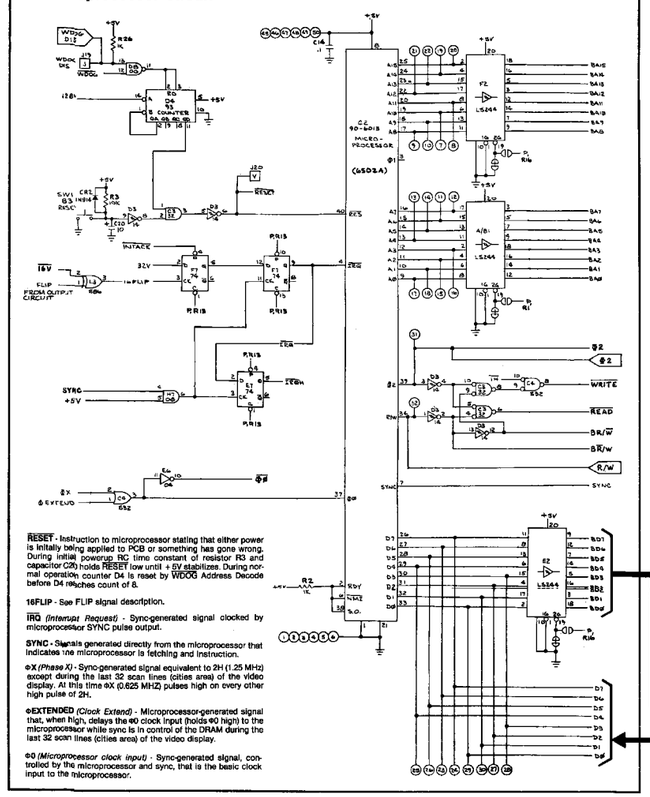
3INH *(Third-color bit Inhibit)* - Sync generated signal that, when high, prohibits a 3rd-color bit output from the Picture Bit Converter circuit in the video output. 3INH goes low during the last 32 scan lines (cities area) of the video display.

$\overline{\text{RAS}}$ *(Row-Address Strobe)* - See Dynarhic RAM (DRAM) Sheet 2, Side A.

DEADSEL *(Address Select)* - See Dynamic RAM (DRAM) Sheet 2, Side A for description of signal.

$\overline{\text{CAS}}$ *(Column-Address Strobe)* - See Dynamic RAM (DRAM) Sheet 2, Side A.

Microprocessor Circuit



$\overline{\text{RESET}}$ - Instruction to microprocessor stating that either power is initially being applied to PCB or something has gone wrong. During initial powerup RC time constant of resistor R3 and capacitor C20 holds $\overline{\text{RESET}}$ low until +5V stabilizes. During normal operation counter D4 is reset by WDOG Address Decode before D4 reaches count of 8.

16FLIP - See FLIP signal description.

$\overline{\text{IRQ}}$ *(Interrupt Request)* - Sync-generated signal clocked by microprocessor SYNC pulse output.

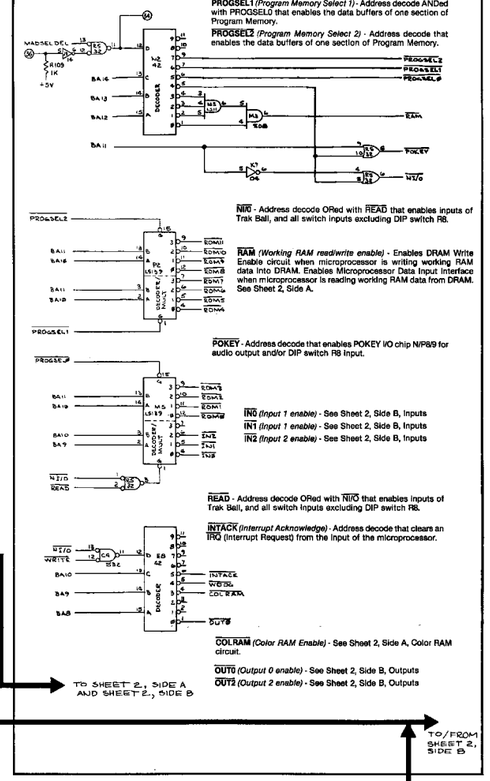
SYNC - Signals generated directly from the microprocessor that indicates the microprocessor is fetching and instruction.

Φ*X (Phase X)* - Sync-generated signal equivalent to 2H (1.25 MHz) except during the last 32 scan lines (cities area) of the video display. At this time Φ*X* (0.625 MHZ) pulses high on every other high pulse of 2H.

Φ**EXTENDED** *(Clock Extend)* - Microprocessor-generated signal that, when high, delays the Φ0 clock input (holds Φ0 high) to the microprocessor while sync is in control of the DRAM during the last 32 scan lines (cities area) of the video display.

Φ0 *(Microprocessor clock input)* - Sync-generated signal, controlled by the microprocessor and sync, that is the basic clock input to the microprocessor.

Address Decoding



PROGSEL0 *(Program Memory Select 0)*- Address decode ANDed with PROGSEL1 that enables the data buffers of one section of Program Memory.

PROGSEL1 *(Program Memory Select 1)* - Address decode ANDed with PROGSEL0 that enables the data buffers of one section of Program Memory.

PROGSEL2 *(Program Memory Select 2)* - Address decode that enables the data buffers of one section of Program Memory.

$\overline{\text{NIO}}$ - Address decode ORed with $\overline{\text{READ}}$ that enables inputs of Trak Ball, and all switch inputs excluding DIP switch R8.

$\overline{\text{RAM}}$ *(Working RAM read/write enable)* - Enables DRAM Write Enable circuit when microprocessor is writing working RAM data into DRAM. Enables Microprocessor Data Input Interface when microprocessor is reading working RAM data from DRAM. See Sheet 2, Side A.

$\overline{\text{POKEY}}$ - Address decode that enables POKEY I/O chip N/P8/9 for audio output and/or DIP switch R8 input.

$\overline{\text{IN0}}$ *(Input 1 enable)* - See Sheet 2, Side B, Inputs

$\overline{\text{IN1}}$ *(Input 1 enable)* - See Sheet 2, Side B, Inputs

$\overline{\text{IN2}}$ *(Input 2 enable)* - See Sheet 2, Side B, Inputs

$\overline{\text{READ}}$ - Address decode ORed with $\overline{\text{NIO}}$ that enables inputs of Trak Ball, and all switch inputs excluding DIP switch R8.

$\overline{\text{INTACK}}$ *(Interrupt Acknowledge)* - Address decode that clears an $\overline{\text{IRQ}}$ (Interrupt Request) from the input of the microprocessor.

$\overline{\text{COLRAM}}$ *(Color RAM Enable)* - See Sheet 2, Side A, Color RAM circuit.

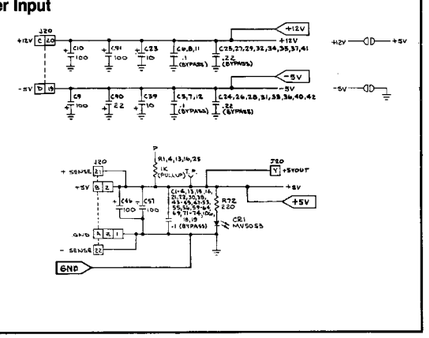
$\overline{\text{OUT0}}$ *(Output 0 enable)* - See Sheet 2, Side B, Outputs

$\overline{\text{OUT2}}$ *(Output 2 enable)* - See Sheet 2, Side B, Outputs

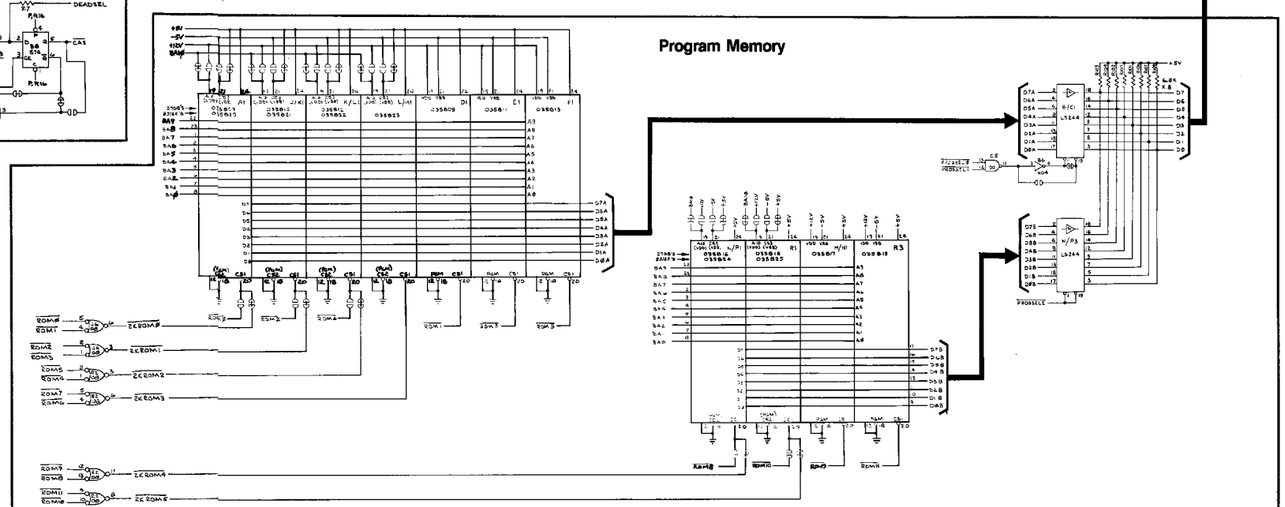
TO SHEET 2, SIDE A AND SHEET 2, SIDE B

TO/FROM SHEET 2, SIDE B

Power Input



Program Memory



Sheet 1, Side B

MISSILE COMMAND™

Microprocessor

Section of 035467-XX D

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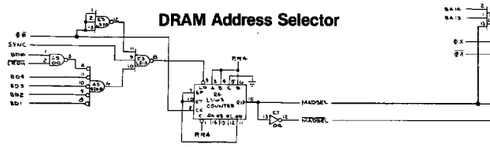
IRQH *(Hardware Interrupt)* - Signal that disables the DRAM Address Controller from putting out a high MADSEL signal.

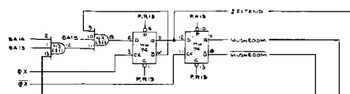
DRAM Address Selector



SYNC - Signal generated directly from the microprocessor that occurs at the beginning of an instruction read cycle and lasts one cycle of microprocessor Φ2 clock. Five Φ0 cycles later, MADSEL goes high.

MADSEL *(Multiplexed Address Select)* - Microprocessor-generated signal that, when high, enables the microprocessor to write or read 2- or 3-color bit data into or out of the DRAM. MADSEL and MUSHROOM together select the address inputs, the data inputs and the actual DRAM chips to be written to or read from. MADSEL also, along with high MUSHROOM and 4X enables the latching of 2-color bit data in the Microprocessor Data Input Interface circuit. See tables in DRAM Write Enable and DRAM Data Input Selector circuits.

3rd Color Bit Select

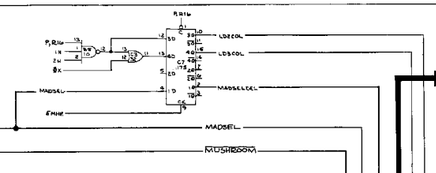


ΦEXTEND *(Clock Extend)* - Microprocessor-generated signal that, when high, delays the Φ0 clock input (holds Φ0 high) to the microprocessor while the microprocessor accesses the 3rd-color bit region of the DRAM.

ΦX *(Phase X)* - Syno-generated signal equivalent to 2H (125 MHz), except during the last 32 scan lines (cities area) of the video display. At this time ΦX pulses high on every other high pulse of 2H (6.625 MHz).

Φ0 *(Microprocessor Clock Input)* - Sync-generated signal, controlled by the microprocessor and sync that is the basic clock input to the microprocessor.

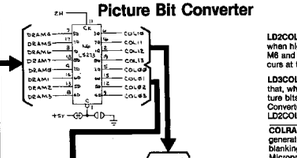
DRAM Picture Output Enable



MUSHROOM	MADSEL	MD0	MD1	MD2	MD3	MD4	MD5	MD6	MD7
LOW	LOW	D7	D6	D5	D4	D3	D2	D1	D0
HIGH	LOW	Invalid State							
LOW	HIGH	D7	D7	D7	D7	D6	D6	D6	D6
HIGH	HIGH	D5	D5	D5	D5	D5	D5	D5	D5

TO SHEET 1, SIDE B
ΦEXTEND → MICROPROCESSOR CIRCUIT

Picture Bit Converter



LD2COL *(Load 2-Color picture bits)* - Sync-generated signal that, when high, loads 2-color parallel picture bits COLX into shifters M6 and N7 of the Picture Bit Converter Circuit. This signal occurs at twice the rate of LD3COL.

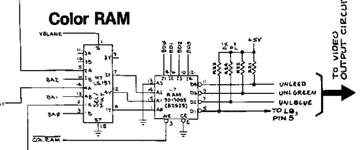
LD3COL *(Load 3rd Color picture bits)* - Sync-generated signal that, when high (SINH must be low) loads 3rd-color parallel picture bits DRAM0 thru DRAM7 into shifter P6 of the Picture Bit Converter Circuit. This signal occurs at one-half the rate of LD2COL.

COLRAM *(Color RAM write enable)* - Color RAM write enable generated by the Address Decoding Circuit. During the vertical blanking period (VBLANK period) COLRAM typically goes low. Microprocessor addresses color RAM L7 with BA0 thru BA2 and writes data into the color RAM on data lines BD0 thru BD3.

COLxx *(2-Color bits)* - Parallel screen bit outputs, from the Picture Bit Converter Circuitry, to shift registers M6 and N7. Bits are latched at output of M6 and loaded into shift resisters M6 and N7 when LD2COL goes low. When LD2COL goes high, serial color bits are clocked out at 5MHz rate.

VBLANK *(Vertical Blanking)* - Syno-generated signal that permits the microprocessor to access the Color RAM and write color commands during the vertical blanking period of the monitor display.

Color RAM



UNLBLUE *(Unlatched Blue color signal)* - Unlatched blue color signal output of Color RAM.

UNLGREEN *(Unlatched Green color signal)* - Unlatched green color signal output of Color RAM.

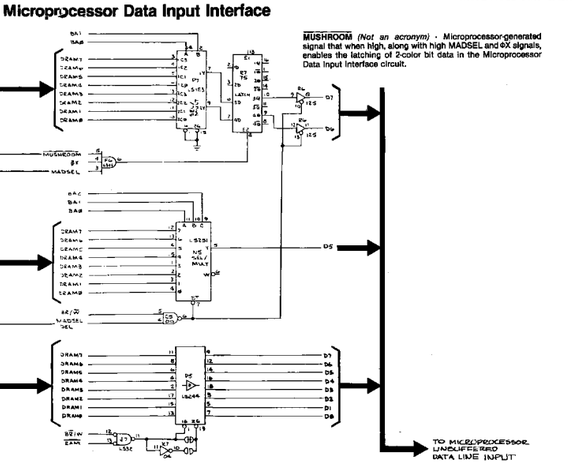
UNLRED *(Unlatched Red color signal)* - Unlatched red color signal output of Color RAM.

SINH *(Third-color bit Inhibit)* - Sync-generated signal that, when high, prohibits a 3rd-color bit output from the Picture Bit Converter circuit. SINH goes low during the last 32 scan lines (cities area) of the video display.

TO VIDEO OUTPUT CIRCUIT
TO LB, PIN 5*

MADSEL — TO SHEET 1, SIDE B ADDRESS DECODING CIRCUIT

Microprocessor Data Input Interface



MUSHROOM *(Not an acronym)* - Microprocessor-generated signal that when high, along with high MADSEL and 4X signals, enables the latching of 2-color bit data in the Microprocessor Data Input Interface circuit.

MADSELDEL *(Multiplexed Address Select Delayed)* -Microprocessor-generated signal delayed one pulse of 5MHz from MADSEL signal. When MADSELDEL is high, along with high BRW, microprocessor reads DRAM data output through Microprocessor Data Input Interface. MADSELDEL also disables Microprocessor Address Decoding Circuit.

BRW *(Buffered Read/Write)* - Microprocessor-generated read/write signal used, along with RAM, to enable data port P5. When enabled, the microprocessor reads the working RAM area of the DRAM on data lines D0 thru D7.

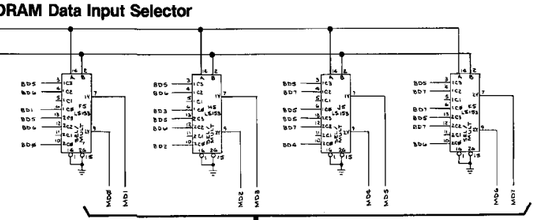
TO MICROPROCESSOR UNBUFFERED DATA LINE INPUT

BR/W *(Buffered Read/Write)* - Microprocessor-generated signal that, when low (see RAM and MADSEL), enables the DRAM Write Enable Circuit to output high write pulses WPx to the DRAM. When high, along with a high MADSELDEL enables picture data to be read from Microprocessor Data Input Interface on data lines D5, D6 and D7.

MUSHROOM *(Not an acronym)* - Microprocessor-generated signal that, when high, enables the microprocessor to write or read the 3rd-color bit data into the DRAM. MUSHROOM and MADSEL together select the address inputs, the data inputs and the actual DRAM chips to be written to or be read from. See tables in DRAM Write Enable and DRAM Data Input Selector circuits.

CAS *(Column Address Strobe)* - Sync-generated strobe that, along with RAS and DEADSEL, sets up the address input to the DRAM. RAS sets up the seven row-address bits and latches the bit inputs for the DRAM row address. CAS sets up the seven column-address bits and latches the bit inputs for the DRAM column address. DEADSEL selects the origin of the seven address-bit inputs.

DRAM Data Input Selector

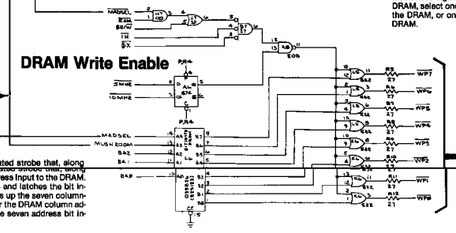


Address Input D-15	WP0	WP1	WP2	WP3	WP4	WP5	WP6	WP7	
16	0	0	1	1	0	1	1	1	2-color bit data
17	1	0	1	1	0	1	1	1	
18	1	1	0	1	1	1	0	1	
19	1	1	1	0	1	1	1	0	
20	0	1	1	1	0	1	1	1	
21	1	0	1	1	1	0	1	1	
22	1	1	0	1	1	1	0	1	
23	1	1	1	0	1	1	1	0	
24	0	1	1	1	1	1	1	1	3rd-color bit data
25	1	0	1	1	1	1	1	1	
26	1	1	0	1	1	1	1	1	
27	1	1	1	0	1	1	1	1	
28	1	1	1	1	0	1	1	1	
29	1	1	1	1	1	0	1	1	
30	1	1	1	1	1	1	0	1	
31	1	1	1	1	1	1	1	0	

WPx *(Write enable Pulses)* - Microprocessor-generated signals that select eight DRAM chips in the working RAM area of the DRAM, select one pair of DRAM chips in the 2-color bit region of the DRAM, or one DRAM chip in the 3rd-color bit region of the DRAM.

MDx *(Multiplexed Data)* - Data line to the DRAM from the microprocessor, selected by MADSEL and MUSHROOM signal. Table DRAM Data Input Selector Circuit defines source, controlled by MADSEL and MUSHROOM signals.

DRAM Write Enable

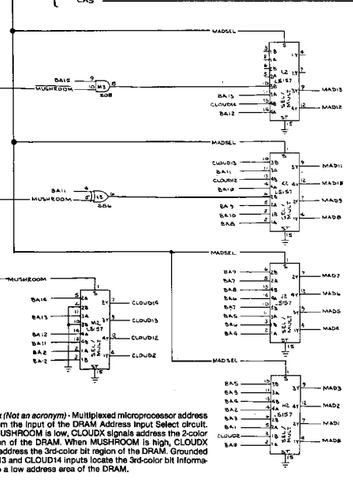


DEADSEL *(Address Select)* - Sync-generated strobe that, along with RAS and CAS, sets up the address input of the DRAM. RAS strobes the DRAM to latch the row-address inputs. CAS strobes the DRAM to latch the column-address inputs. When high, DEADSEL selects the row-address inputs. When low, DEADSEL selects the column-address inputs.

RAS *(Row Address Strobe)* - Sync-generated strobe that, along with CAS and DEADSEL, sets up the address input to the DRAM. RAS sets up the seven row address bits and latches the bit inputs for the DRAM row address. CAS sets up the seven column-address bits and latches the bit inputs for the DRAM column address. DEADSEL selects the origin of the seven address bit inputs.

FROM SYNC CIRCUIT: RAS, DEADSEL, CAS

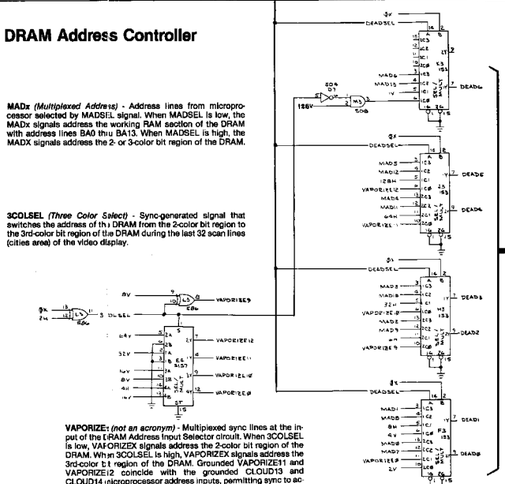
DRAM Address Controller



MADx *(Multiplexed Address)* - Address lines from microprocessor selected by MADSEL signal. When MADSEL is low, the MADx signals address the working RAM section of the DRAM with address lines BA0 thru BA13. When MADSEL is high, the MADX signals address the 2- or 3-color bit region of the DRAM.

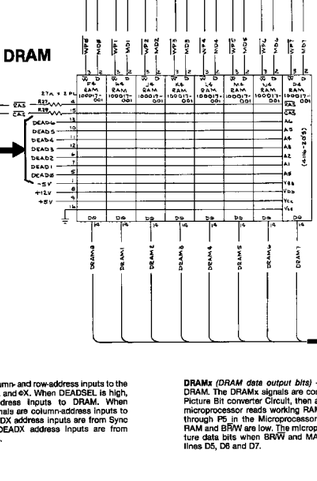
3COLSEL *(Three Color Select)* - Sync-generated signal that switches the address of the DRAM from the 2-color bit region to the 3rd-color bit region of the DRAM during the last 32 scan lines (cities area) of the video display.

CLOUDx *(Not an acronym)* - Multiplexed microprocessor address lines from the input of the DRAM Address Input Select circuit. When MUSHROOM is low, CLOUDX signals address the 2-color bit region of the DRAM. When MUSHROOM is high, CLOUDX signals address the 3rd-color bit region of the DRAM. Grounded CLOUD13 and CLOUD14 inputs locate the 3rd-color bit Information into a low address area of the DRAM.



VAPORIZEx *(not an acronym)* - Multiplexed sync lines at the input of the DRAM Address Input Selector circuit. When 3COLSEL is low, VAPORIZEX signals address the 2-color bit region of the DRAM. When 3COLSEL is high, VAPORIZEX signals address the 3rd-color bit region of the DRAM. Grounded VAPORIZE11 and VAPORIZE12 coincide with the grounded CLOUD13 and CLOUD14 microprocessor address inputs, permitting sync to access the 3rd-color bit information in the low address area of the DRAM.

DRAM



DEADx *(DRAM Address)* - Column- and row-address inputs to the DRAM selected by DEADSEL and 4X. When DEADSEL is high, DEADX signals are row-address inputs to DRAM. When DEADSEL is low, DEADX signals are column-address inputs to DRAM. When 4X is low, DEADX address inputs are from Sync Circuit. When 4X is high, DEADX address inputs are from microprocessor address lines.

DRAMx *(DRAM data output bits)* - Data output bits from the DRAM. The DRAMx signals are converted to serial data by the Picture Bit converter Circuit, then address the Color RAM. The microprocessor reads working RAM data DRAM0 thru DRAM7 through P5 in the Microprocessor Data Input Interface when RAM and BRW are low. The microprocessor reads selected picture data bits when BRW and MADSELDEL are high on data lines D5, D6 and D7.

ATARI®

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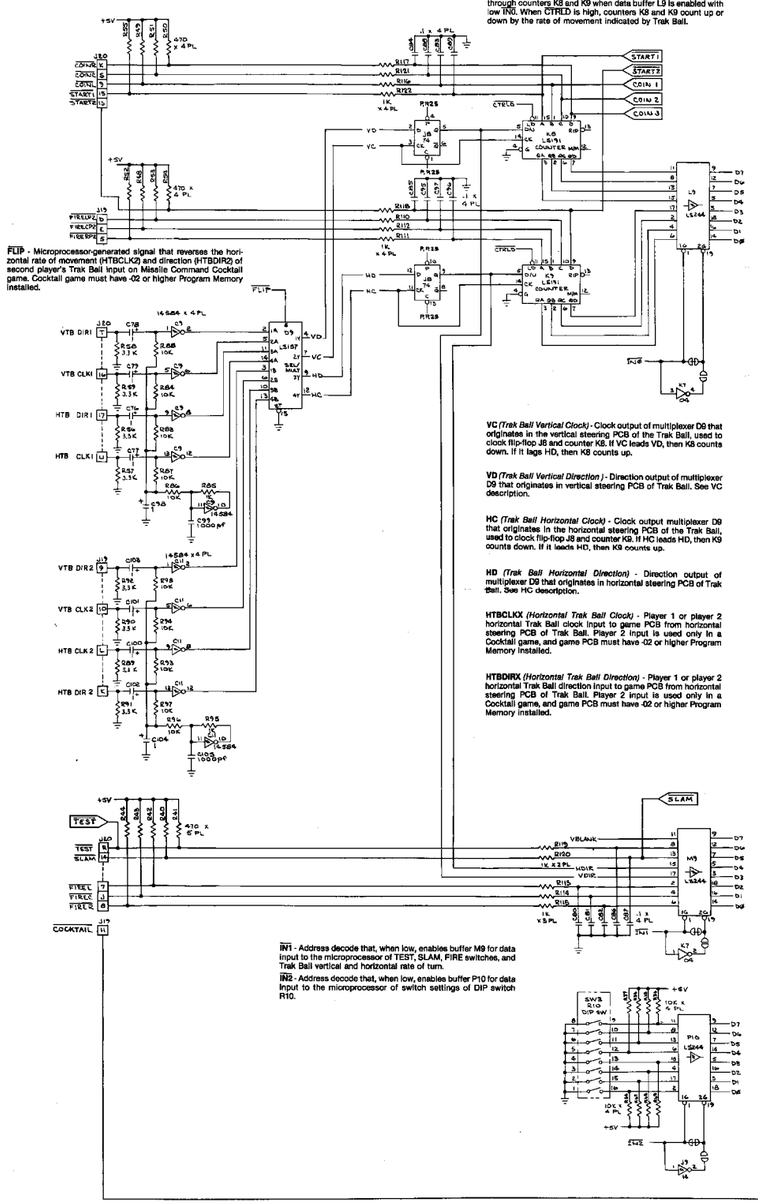
Sheet 2, Side A

MISSILE COMMAND™

Video Generator

Section of 035467-XX D

Input Circuits



CTRLD *(Counter load enable)* - Latched microprocessor output that, when low, permits microprocessor to read switch data through counters K8 and K9 when data buffer L9 is enabled with low **IN0**. When **CTRLD** is high, counters K8 and K9 count up or down by the rate of movement indicated by Trak Ball.

FLIP - Microprocessor-generated signal that reverses the horizontal rate of movement (HTBCLK2) and direction (HTBDIR2) of second player's Trak Ball input on Missile Command Cocktail game. Cocktail game must have -02 or higher Program Memory installed.

VC *(Trak Ball Vertical Clock)* - Clock output of multiplexer D6 that originates in the vertical steering PCB of the Trak Ball, used to clock flip-flop J8 and counter K8. If VC leads VD, then K8 counts down. If it lags HD, then K8 counts up.

VD *(Trak Ball Vertical Direction)* - Direction output of multiplexer D9 that originates in vertical steering PCB of Trak Ball. See VC description.

HC *(Trak Ball Horizontal Clock)* - Clock output multiplexer D9 that originates in the horizontal steering PCB of the Trak Ball, used to clock flip-flop J8 and counter K9. If HC leads HD, then K9 counts down. If it leads HD, then K9 counts up.

HD *(Trak Ball Horizontal Direction)* - Direction output of multiplexer D9 that originates in horizontal steering PCB of Trak Ball. See HC description.

HTBCLKX *(Horizontal Trak Ball Clock)* - Player 1 or player 2 horizontal Trak Ball clock input to game PCB from horizontal steering PCB of Trak Ball. Player 2 input is used only in a Cocktail game, and game PCB must have -02 or higher Program Memory installed.

HTBDIRX *(Horizontal Trak Ball Direction)* - Player 1 or player 2 horizontal Trak Ball direction input to game PCB from horizontal steering PCB of Trak Ball. Player 2 input is used only in a Cocktail game, and game PCB must have -02 or higher Program Memory installed.

IN1 - Address decode that, when low, enables buffer M9 for data input to the microprocessor of TEST, SLAM, FIRE switches, and Trak Ball vertical and horizontal rate of turn.

IN2 - Address decode that, when low, enables buffer P10 for data input to the microprocessor of switch settings of DIP switch R10.

Memory Map for Address Decoding Circuit, Sheet 1, Side B

MEMORY MAP

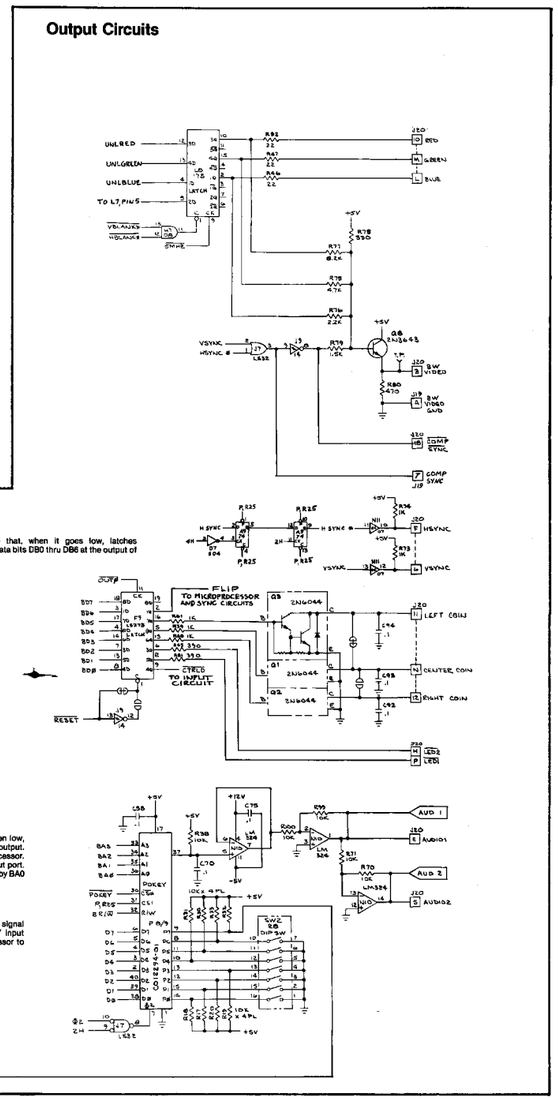
	ADDRESS																DATA								
HEXIDECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-01FF	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	512 Bytes of Working RAM
0200-05FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	3rd-color-bit region of Screen RAM
0600-063F	0	0	0	0	0	1	1	0	0	0	A	A	A	A	A	A		D	D	D	D	D	D	D	D	More Working RAM
06F0-3FFF	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A		D	D	D	D	D	D	D	D	3-color-bit region of Screen RAM
4000-400F	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	POKEY Ports
4800	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D								Right Coin Switch Input
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R		D							Center Coin Switch Input
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R			D						Left Coin Switch Input
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R				D					1-player Start Switch Input
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R					D				2-player Start Switch Input
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R						D			2nd-player left Fire Switch Input (Cocktail Only)
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R							D		2nd-player center Fire Switch Input (Cocktail Only)
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R								D	2nd-player right Fire Switch Input (Cocktail Only)
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R						D	D	D	Horizontal TRAK BALL displacement if CTRLD latched high
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D					Vertical TRAK BALL displacement if CTRLD latched high
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W				D					Screen Flip
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W			D						Left Coin Counter Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W				D					Center Coin Counter Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W					D				Right Coin Counter Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W						D			2-Player Start LED Output
	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	W							D		1-Player Start LED Output
4900	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	W								D	**CTRLD** - If low, read Switches. If high, read TRAK BALL
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R	D								VBLANK read
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R		D							Self-Test Switch Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R			D						SLAM Switch Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R				D					Horizontal TRAK BALL Direction Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R					D				Vertical TRAK BALL Direction Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R						D			1st-player left Fire Switch Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R							D		1st-player center Fire Switch Input
	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	R								D	1st-player right Fire Switch Input
4A00	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	D	Option Switch Inputs
4B00-4B07	0	1	0	0	1	0	1	1	0	0	0	0	0	0	A	A	W					D	D	D	D	Color RAM
4C00	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	W									Watchdog
4D00	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	W									Interrupt Acknowledge
5000-7FFF	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	Program

VB CLKX *(Vertical Trak Ball Clock)* - Player 1 or player 2 vertical Trak Ball clock input to game PCB from vertical steering PCB of Trak Ball. Player 2 input is used only in Cocktail game, and game PCB must have -02 or higher Program Memory installed.

VB DIRX *(Vertical Trak Ball Direction)* - Player 1 or player 2 vertical Trak Ball direction input to game PCB from vertical steering PCB of Trak Ball. Player 2 input is used only in Cocktail game, and game PCB must have -02 or higher Program Memory installed.

IN0 - Address decode that, when low, enables buffer L9 for data input to the microprocessor of COIN switches, START switches, player 2 FIRE switches (for Cocktail game only), or Trak Ball rate of turn information. If **CTRLD** is low, data is from switches. If high, Data is Trak Ball Information.

Output Circuits



OUT0 - Address decode that, when it goes low, latches microprocessor-buffered data bits D80 thru D86 at the output of latch F9.

POKEY *(POKEY chip enable)* - Address decode that, when low, enables custom I/O POKEY chip N/P9/9 for data input or output. The POKEY chip works in conjunction with the microprocessor. It is the input port for DIP switch R8 and the audio output port. **BRW** determines the direction of data flow as addressed by BA0 thru BA3.

BRW *(Buffered Read/Write)* - Microprocessor-generated signal that, when high, allows microprocessor to read POKEY input data from DIP switch R8. When low, allows microprocessor to write to POKEY output.

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Sheet 2, Side B

MISSILE COMMAND™

Input and Output Circuitry

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DP-150-02 1st printing