SPECTAR TECHNICAL MANUAL

Exidy

1.1

SPECTAR (TM)

Technical Manual 1.1

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FOREWARD

This manual is designed for your ease in reading schematics. A description accompanies each schematic on the opposite page. This should help clarify the schematics and aid in your understanding of the technical aspects of SPECTAR.

The following is an outline of the information contained in the schematic descriptions: To find the particular information you are interested in, look up the schematic PAGE number as listed, and opposite the schematic is additional verbal explanation.

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3. Processor Workspace RAM (4A, 5A)
4. Main Address Decoding (5C, 5D, 5E)

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3. Memory Device "Personality" Selection (11B)

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APPENDIX A: PARTS LIST FOR SPECTAR

SCHEMATICS

GAME LOGIC PCB

1. **Master Oscillator (1D)**
   From this oscillator all dynamic operations are derived, such as the processor clock, the main element and line counters, the shift register clocks, as well as all other forms of timing signals.

2. **Element (Horizontal) Counters (1C, 1E, 2E)**

   These components form the final stages of horizontal timing. All operations in this game requiring horizontal positioning or timing have their origin here. Note that, beginning with signal HCLK (from Clock Divide Counter 2D), there are 256 counts prior to setting signal E256 high. When this signal goes high, it indicates that the horizontal blanking period is in progress. At this time the final counter (1E) is preloaded with a higher number than previously loaded. This creates a shorter count the second time around. The shorter count measures the retrace interval. When the retrace count is finished, the counter preloads with a lower number, establishing a longer count sequence again for "real time" sweep of the electron beam across the face of the CRT.

3. **Line (Vertical) Counters (4F, 5F, 6E)**

   These components form the entire vertical timing operation starting with a clock derived from horizontal timing. These counters count 256 times and then preload with a higher number, causing a shorter count the second time. This shorter count measures the vertical retrace interval. Note that signal L256, when high, indicates vertical blanking is in progress. After the completion of the vertical retrace count, the counters once again preload with a lower number. This way they count 256 times during the sweep of the electron beam down the face of the CRT, allowing the horizontal timers to sweep one complete horizontal line for each count of the vertical counters. Thus, the electron beam reaches the bottom of the CRT, after completing 256 horizontal line sweeps. It then begins the vertical retrace count, and the whole cycle begins anew with the beam starting again at the top of the CRT.

4. **Screen RAM Addresses (7D)**

   During the time the screen RAM is examined by the logic for output to the monitor screen, addresses must be applied to the screen RAM to count up at a rate corresponding to the image cells conceptually arranged on the screen in a 32 x 32 matrix. The counts used here, 4 from the element counters, and 4 from the line counters, fulfill this timing requirement. The least significant element count used (E8) represents an interval exactly eight times that of one element. The least significant line count used represents an interval exactly eight times that of one horizontal line, or eight times a single line count. Dividing a 256 element line by 8 yields 32, and likewise dividing a 256 line vertical sweep by 8 yields 32. Thus the screen RAM address lines (RAM0 through RAM9) count at a rate that creates 32 horizontal counts and 32 vertical counts as the electron beam sweeps the face of the CRT. This makes 1024 conceptual "image cells" into which can then be inserted images of 8 elements by 8 lines. For more information concerning these images, refer to the text for page 3 of the Logic Schematics.

5. **Coin Input Decoding (1H)**

   Some models of SPECTAR contain two separate coin inputs for special coinage applications. NOR gate 1H combines these separate inputs, making signal 5COINT, which sets the interrupt flip-flop (6E on page 8) when either coin input becomes active, thus forcing the microprocessor to jump the interrupt service routine. This interrupt driven operation prevents ever missing a coin when inserted. However, this also means that when a game is first powered up, the coin input must be inactive. If for some reason the coin input switch is enabled at the time of power up, the game does not properly initialize until the switch is disabled.

6. **Hardware Generated Line Positioning Proms (3E, 4E)**

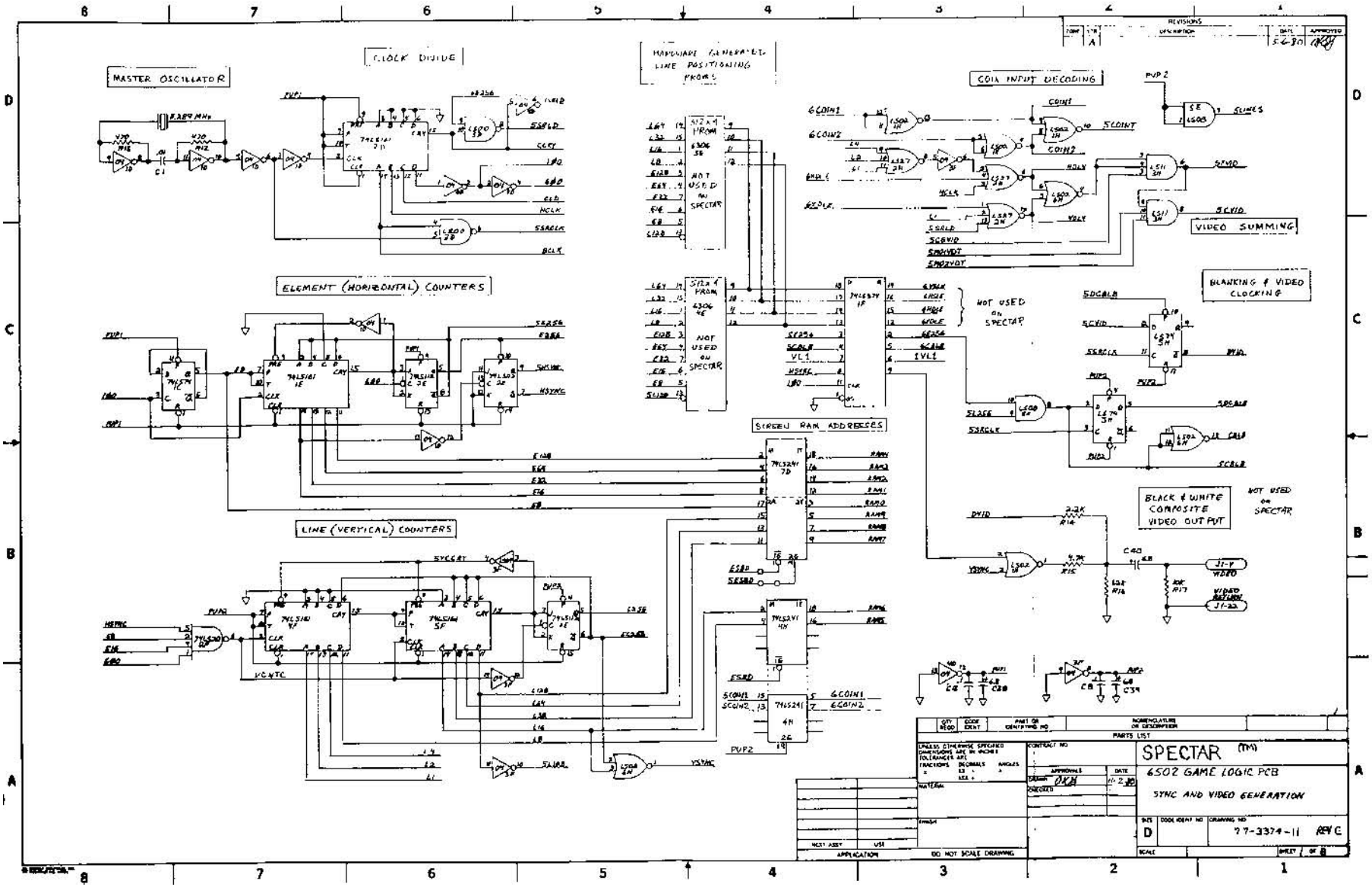
   These PROMs are not used for SPECTAR. Generally their function is to create solid or dotted lines on the screen.

7. **Blanking and Video Clocking (5H)**

   Flip-flop 5H merely combines blanking and all other video.

8. **Black and White Composite Video Output (1H)**

   This circuit is not used for SPECTAR. If desired, however, these components may be installed to aid troubleshooting, by acting as a "video probe".


MASTER OSCILLATOR
CLOCK DIVIDE
HARDWARE GENERATED LINE POSITIONING PROMS
COIN INPUT DECODING
VIDEO SUMMING
ELEMENT (HORIZONTAL) COUNTERS
BLANKING & VIDEO CLOCKING
SCREEN RAM ADDRESSES
NOT USED ON SPECTAR
LINE (VERTICAL) COUNTERS
BLACK & WHITE COMPOSITE VIDEO OUTPUT
NOT USED ON SPECTAR
SPECTAR (TM)
6502 GAME LOGIC PCB
SYNC AND VIDEO GENERATION
77-3374-11 REV C
DO NOT SCALE DRAWING

GAME LOGIC PCB

1. **Screen Controller PROM (6D)**

   This PROM controls the direction of data flow into and out of the screen RAM and character generator RAM. It prevents timing errors and buss conflicts, assuring that the microprocessor can write to either the screen or character generator RAM, or read back from either.

2. **Screen RAM (7B, 8B)**

   The screen RAM is comprised of two 1024 x 4 static RAMs, configured to act as a single 1024 x 8 RAM. This creates a screen matrix of 32 horizontal by 32 vertical positions. A single byte code is stored in each of these positions to represent a particular character. During "real time" (the time the CRT is being swept by the electron beam) these character codes address the character generator RAM. Note that the PCB could substitute PROM for character generator RAM, but is not so configured for SPECTAR.

   These character codes, when used as addresses, are combined with the three least significant line counts (L1, L2, L4) to present to the character generator output shift register all the necessary data to form an 8 element wide by 8 line high character on the CRT, located within one of the 1024 positions mentioned immediately above, that is, the 32 horizontal by 32 vertical positions.

   The screen, then, is a storage place for single byte codes that call up an 8 x 8 character and place it into the corresponding character cell. This character is stored in the character generator RAM, shown on page 3 of the schematic.

3. **Character Image Storage**

   Shown on this page are two PROMs (9C, 10C). They could be used as a permanent set of characters. However, SPECTAR uses RAM instead, to increase the flexibility in character manipulation. This portion of RAM appears on page 3 of the Logic schematics.

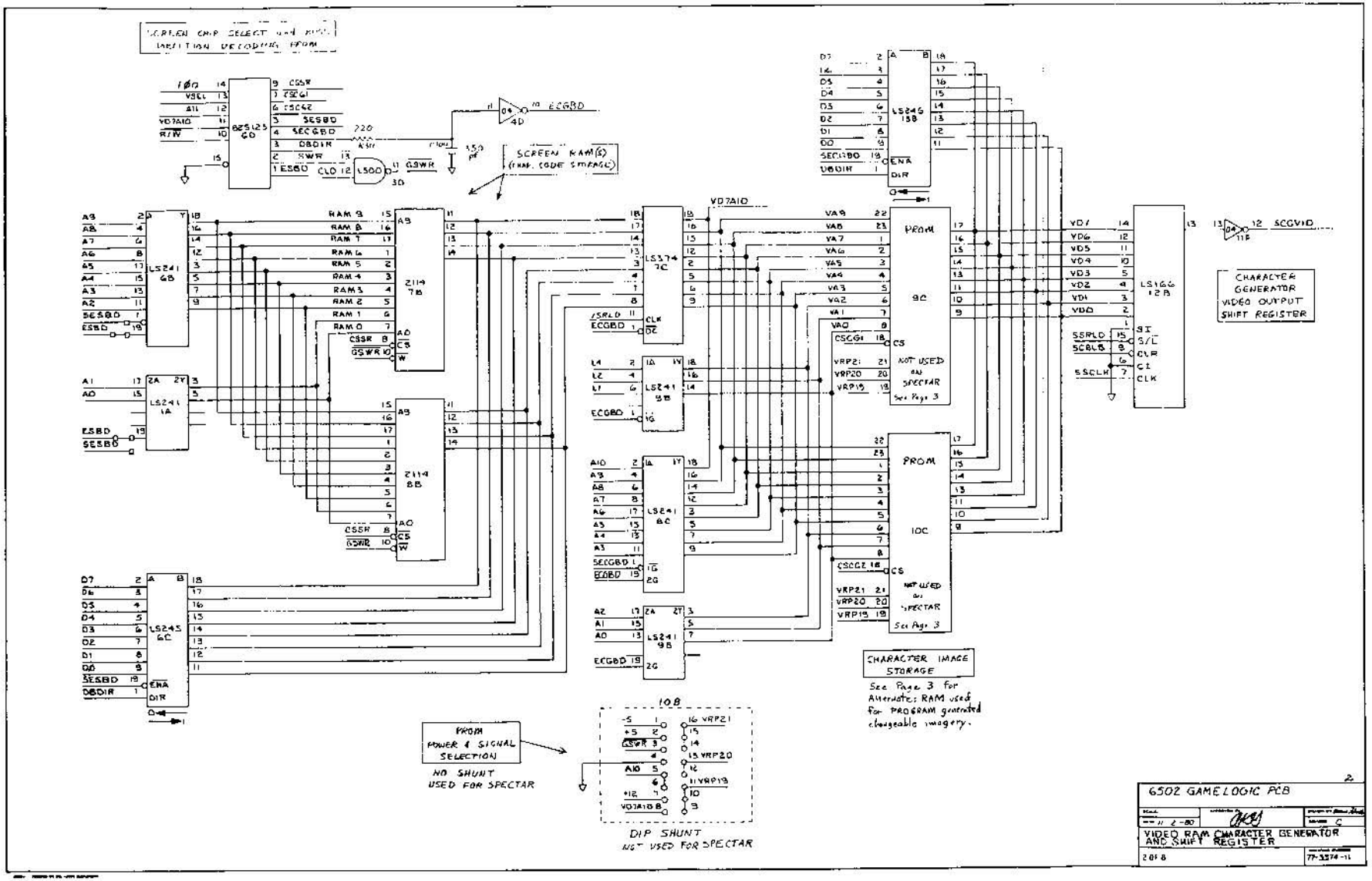
4. **PROM Power and Signal Selection (10B)**

   This Dip Shunt configures the logic for different types of PROM devices. For SPECTAR, however, this Dip Shunt is unnecessary due to the fact that RAM has been used rather than PROM.

5. **Character Generator Output Shift Register (12B)**

   Video from the character generator memory devices (RAM in the case of SPECTAR) is formed by this shift register as a byte of data that displays one line at a time from left to right on the CRT. This ultimately forms an 8 line high by 8 element wide character positioned on the screen according to the time it is presented to the shift register.

   Output from this shift register is all the images seen on the screen except the player image and the player missile image.


SCREEN CHIP SELECT AND R/W DECODING FROM ADDRESS DECODING PROM
SCREEN RAM (6) (CHAR. CODE STORAGE)
VD7A10
ECGBD
SCGVID
CHARACTER GENERATOR VIDEO OUTPUT SHIFT REGISTER
CHARACTER IMAGE STORAGE
See Page 3 for Alternate: RAM used for PROGRAM generated changeable imagery.
PROM POWER & SIGNAL SELECTION
NO SHUNT USED FOR SPECTAR
DIP SHUNT NOT USED FOR SPECTAR
NOT USED on SPECTAR
See Page 3
6502 GAME LOGIC PCB
VIDEO RAM CHARACTER GENERATOR AND SHIFT REGISTER
2 OF 8
77-3574-11

GAME LOGIC PCB
Image Storage RAM

1. **Character Generator Image Storage RAM (13C, 11C, 14C, 12C)**

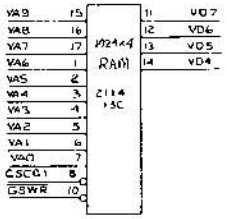
   These four RAMs, when used in this configuration, act as a 2048 x 8 bit RAM. The images placed on the screen are stored in this RAM by the microprocessor, according to the game program. In this RAM images are established, altered, shifted slightly, and even replaced with a new set, if required by the program.

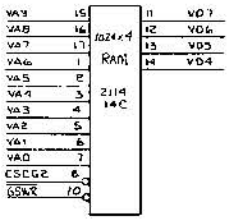
   When called by the logic to do so, the RAM presents, to the character generator shift register, a single byte, representing one line of a particular image. Each image is composed of 8 lines of data, each line is one byte-wide. Thus, 256 images of 8 x 8 bits can be stored here simultaneously and "called up" by the screen RAM to be displayed on the CRT in any of the 1024 character cell positions. A single byte code, stored in the screen RAM, calls up a character. The character may change or move by replacing the single byte code in the screen RAM, or by altering the data in the character generator RAM which forms the image.

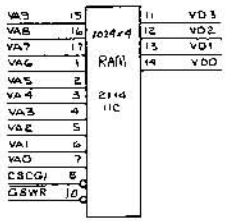
MASTER ORGANIZATION
IMAGE STORAGE RAMS

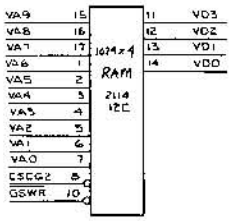
For use with PROGRAM generated designable masters.

USED on SPEED FREAK









3

6502 GAME LOGIC PCB

SCALE	APPROVED BY AKB	SIZE C
DATE 11-2-80		

IMAGE STORAGE RAM

3 OF 8	11-3329-11

GAME LOGIC PCB

1. **The 6502 Microprocessor (2A)**

   For detailed information concerning this microprocessor, refer to the MOSTEK publication, 6500-10A, MCS Microcomputer Family Hardware Manual.

   One feature that should be mentioned here, however, is that this microprocessor has "memory-mapped I/O". This means that all ports interfacing to peripherals of any type must be located within the normal memory map, with no duplication of addresses, since no instructions are specifically oriented toward I/O operations.

2. **Power-on Reset circuit (connected to 2A pin 40)**

   When power is first applied to a game, a particular sequence f events must occur to set up all logic conditions. If this sequence is broken for what ever reason, the microprocessor may become confused, and the game will not start and run.

   This sequence is accomplished when the reset line to the microprocessor is the last line allowed to reach a "high" logic level. The Power-on reset circuit makes sure this occurs by utilizing the charge time of an RC network as a delay.

   If any kind of power interruption occurs during normal game play, the power-on reset circuit insures that the microprocessor is reset. This alleviates thoroughly confusing the microprocessor while it also recreates the original power- on sequence.

3. **Processor Workspace RAM (4A, 5A)**

   The RAM, or workspace, consists of the lowest 1024 bytes of memory and can be divided into three separate sections due to distinctly different functions.

   The lowest 256 bytes (0 to FF Hexadecimal) is reserved for special software register operations, and is called "zero page". The processor uses this area to store dynamic variables. For details of this type of operation, refer to 6502 technical literature regarding "Zero Page Addressing".

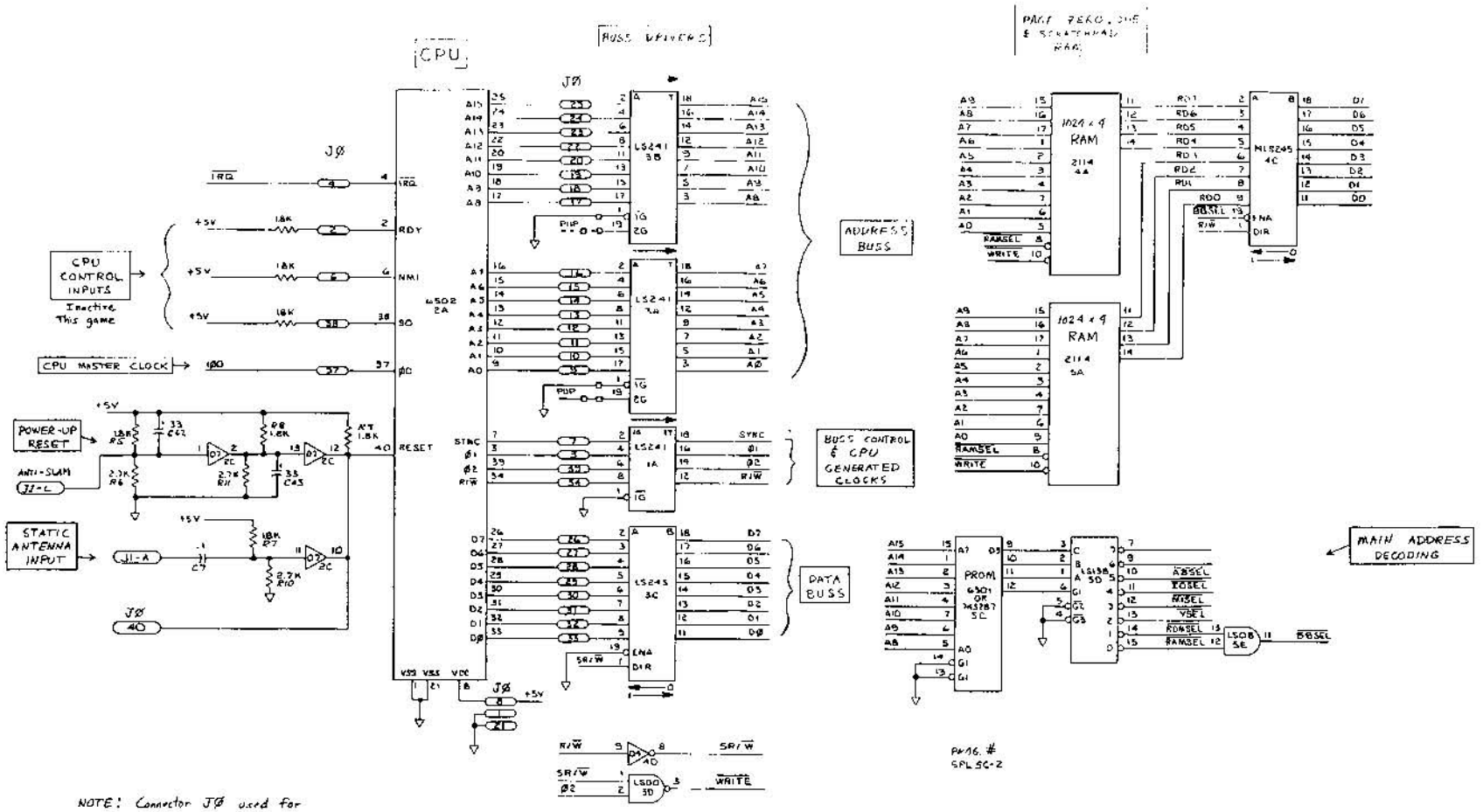
   The next higher 256 bytes (100 to 1FF Hex) is reserved for the 6502 stack. The processor stores return addresses in the stack when interrupted or called to execute a subroutine. The game program may also request the processor to store other kinds of information here for later retrieval.

   The next higher 512 bytes (200 to 3FF Hex) are used as a scratchpad area. Miscellaneous calculations and their results are temporarily stored here.

4. **Main Address Decoding (5C, 5D, 5E)**

   This circuit is the first stage of the address line decoding necessary to organize the memory map; that is, it places specifi functions or devices within generalized blocks of the memory map, grouped by function.

   For details on the addressing scheme, see MEMORY MAP, Figure 1.


CPU
BUSS DRIVERS
PART PERO. SHT & SCRATCHPAD RAM
J0
IRQ
+5V
1.8K
RDY
NMI
SO
CPU CONTROL INPUTS
Inactive This game
CPU MASTER CLOCK
Ø0
RESET
POWER-UP RESET
ANTI-SLAM
J1-L
STATIC ANTENNA INPUT
J1-A
J0 40
6502 2A
LS241 3B
LS241 3A
LS245 3C
ADDRESS BUSS
BUSS CONTROL & CPU GENERATED CLOCKS
DATA BUSS
SYNC
Ø1
Ø2
R/W
SR/W
WRITE
1024 x 4 RAM 2114 4A
1024 x 4 RAM 2114 5A
MLS245 4C
PROM 6301 OR MS7287 5C
LS138 5D
LS08 5E
MAIN ADDRESS DECODING
ABSEL
BOSEL
RDSEL
WRSEL
VSEL
RAMSEL
BBSEL
DIR
ENA
PROM #
SPL SC-2
NOTE: Connector J0 used for test & analysis purposes only. Contains all CPU connections.
4
6502 GAME LOGIC PCB
11-2-80
RESET: CONT. PROGRAM RAM BUS ARCHITECTURE
4 OF 8
11-5574-11

GAME LOGIC PCB

1. **Program Memory (6A through 13A)**

   These memory devices are 2716 EPROMS on Spectar. Note that four of the lines to each memory device (PC$0 through PC$7, PAP19, PAP20, PAP21) are programmable through jumper configurations located at 4B and 11B. This allows different memory devices to be used and/or it relocates the program memory within the memory map.

   CAUTION

   Some Spectar boards are configured for 2716 EPROMS needing only a single +5v supply, while others are configured for EPROMS requiring +12v, +5v, and -5v. REPLACING EPROMS without due regard to this configuration may destroy all program memory devices. If in doubt, please first contact the Exidy Service Department for assistance.

2. **PROM Address Selection (4B, 5B)**

   This is a second stage of address decoding, used to select each individual memory device when addressed. Signal ROMSEL (from page 4 Main Address Decoding) selects the Program Memory devices in general, and jumper 4B, together with decoder 5B further defines an address to a particular memory device.

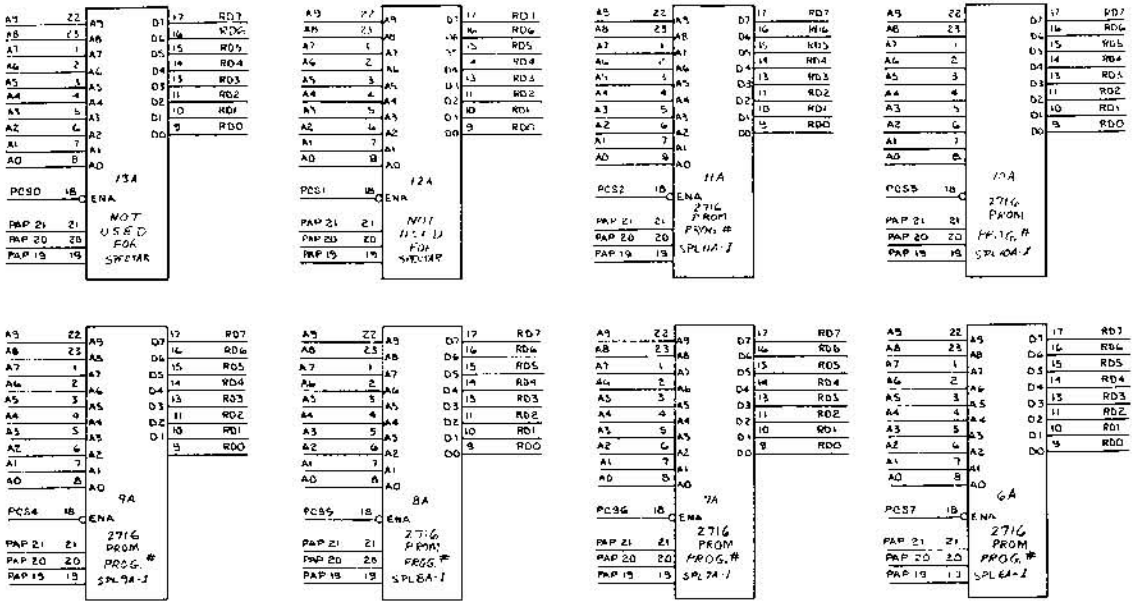
3. **Memory Device "Personality" Selection (11B)**

   The dip shunt, or jumpers block, alters power and signal configuration to the program memory devices. Note that the configuration shown on the schematic requires the use of 2716 EPROMS needing +12v, +5v, and -5v. PLEASE EXERCISE CAUTION regarding any change, in this configuration or replacement of memory devices.

MEMORY MAP

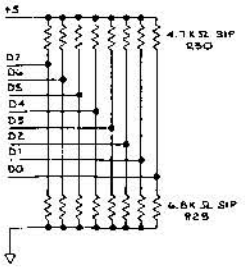
Hex Address	Function or Device
FFF7-FFFF	Interrupt and Reset Vectors
5201	Audio Board Tone Data Latch (write)
5200	Audio Board Control Latch (write)
5103	Interrupt Condition Latch (read)
5101	Control Inputs Port (read)
5101	Output Control Latch (write) (Not used in Spectar upright)
5100	Moving Objects Image Latch (write)
5100	Option Dipswitch Port (read)
50C0	Moving Object 2 Vertical Position Latch (write)
5080	Moving Object 2 Horizontal Position Latch (write)
5040	Moving Object 1 Vertical Position Latch (write)
5000	Moving Object 1 Horizontal Position Latch (write)
4800-4FFF	Character Generator RAM
4000-43FF	Screen RAM
0800-3FFF	Program PROM
0200-03FF	Scratchpad RAM
0100-01FF	Stack RAM
0000-00FF	Zero Page RAM

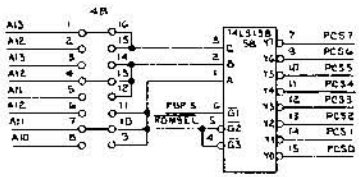
PROGRAM MEMORY



DATA BUSS TERMINATION

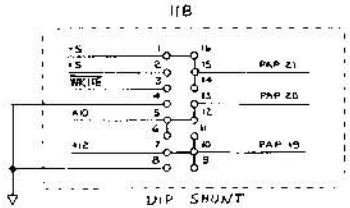
Ringing Suppression





PROM ADDRESS SELECTION

Configuration shown For SPECTAR



MEMORY DEVICE PERSONALITY SELECTION

Configuration shown For "3 VOLTAGE" 2716 EPROM

5

EXIDY INC.

6502 GAME LOGIC PCB CPU ROM

SAFB

GAME LOGIC PCB

1. **Moving Object Horizontal Position (13F, 15F, 14F, 16F)**

   Counters 13F and 15F form a 2 byte-wide counter which horizontally positions Moving Object 1 on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of the Horizontal Sync, they begin to count. The count outputs AND'ed through 15E give rise to signal M1HW, the Horizontal Position Window for Moving Object 1. Counters 14F and 16F are the equivalent circuit for Moving Object 2.

2. **Moving Object Vertical Position Counters (16E, 12E, 1E, 13E)**

   Counters 16E and 12E form a 2 byte-wide counter which positions Moving Object 1 vertically on the screen. These counters are preloaded to a certain value by the microprocessor during Vertical Retrace time. Then, after each occurrence of Vertical sync, they begin counting. The four count outputs of the least significant of these two counters (M1L1, M1L2, M1L3, M1L4) are sent to the moving object image PROM to specify which line of the image is presently being displayed. The AND'ed outputs of the second counter give rise to signal M1VW, the Vertical Position Window for Moving Object 1. Counters 11E and 13E are the equivalent circuit for Moving Object 2.

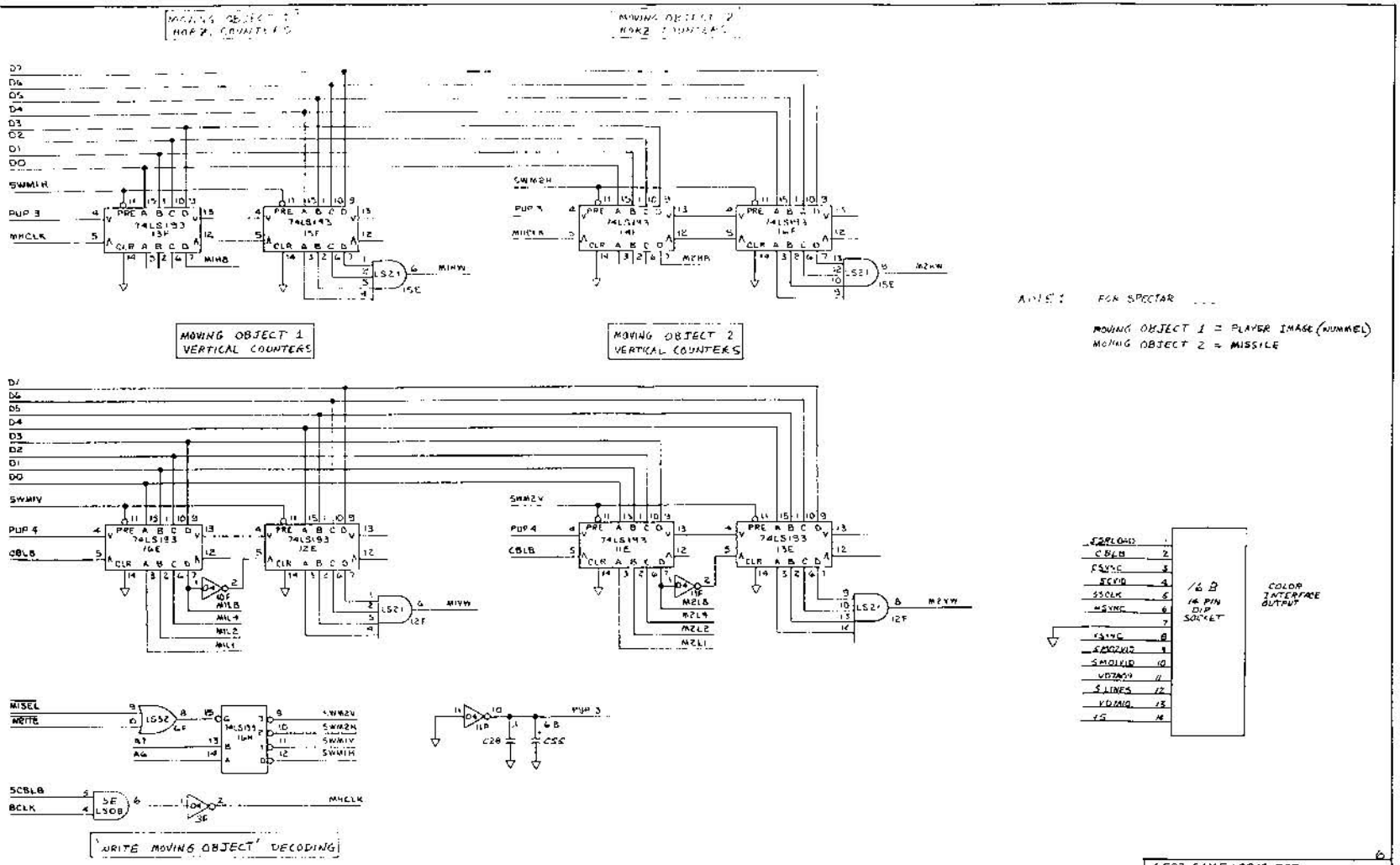
3. **"Write Moving Object" Decoding (6F, 16H, 5E, 3F)**

   Consists of two distinctly different functions. 6F and 16H form the circuit that generates the load pulses for the moving object position counters, while 5E and 3F simply prevent the counters from counting during blanking.

4. **Color Interface Output (16B)**

   This is a 14 pin DIP socket used as the connector interface to the color adapter board. The signals and their functions are:

Pin #		
1	5SRLOAD	= Shift Register Load Pulse (Neg. True)
2	CBLB	= Composite Blanking
3	CSYNC	= Composite Sync
4	5CVID	= Composite Video (Neg. True)
5	5SCLK	= Shift Register CLock (Neg. True)
6	HSYNC	= Horizontal Sync
7	GND	
8	VSYNC	= Vertical Sync
9	5MO2VID	= Moving Object 2 Video (Neg. True)
10	5MO1VID	= Moving Object 1 Video (Neg. True)
11	VD7A09	= Character Generator Address Line 9
12	5LINES	= NOT USED ON SPECTAR
13	VD7A10	= Character Generator Address Line 10 +5V



6

6502 GAME LOGIC PCB

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COLOR INTERFACE OUTPUT AND MOVING OBJECT POSITION COUNTERS

6 OF 8

37-9534-11

GAME LOGIC PCB

1. **Moving Object Multiplexing (14A, 14E)**

   These two multiplexers pass information to the moving objects image PROM. They contain two codes: one determines which image should appear, and the other specifies which line of that image is to be displayed.

   The data passed alternates between data for Moving Object 1 (player image) and Moving Object 2 (player missile), depending on the state of element count E32.

   The upper multiplexer (14A) passes the "which image" code, and the lower multiplexer (14E) passes the "which line of that image" code.

2. **Moving Objects Image PROM (11D)**

   This PROM accepts as data the image and line codes of moving objects 1 and 2 (see "Moving Object Multiplexing" above). It then presents the appropriate data for one line of the image to the output shift registers.

   The timing of the logic insures that the correct pair of shift registers are loaded with the data, then shifted out at the correct time to become, one line at a time, the 16 lines of video for that character (Moving Object 1 or 2).

3. **Moving Object Video Output Shift Registers (12D, 13D, 14D, 15D)**

   Shift registers 12D and 13D together form a 16 bit shift register whose task is to accept, as data, 16 bits (2 bytes) representing a single line of the image for Moving Object 1, then shift these 16 parallel bits out serially to become video. This operation is repeated for 16 consecutive lines, resulting in a video image that is 16 bits wide by 16 lines high on the monitor screen.

   Shift registers 14D and 15D together form this same type of circuit, identical in function, for Moving Object 2.

4. **Moving Objects Shift Register Load Logic (2F, 16H)**

   This circuit sends properly timed load signals to the Moving Object Video Shift Registers. These load signals are needed to load the image data into the shift registers at location 12D or 14D.

5. **Moving Object Shift Register Control Logic (15H, 14H)**

   The input signals to the upper two gates (15H) represent horizontal and vertical position "windows" for the two moving objects (for example, M1HW Moving Object 1 Horizontal Window, M2VW Moving Object 2 Vertical Window). These windows allow the Moving Object shift registers to shift only at the right time. This insures the image is generated at the correct position on the screen.

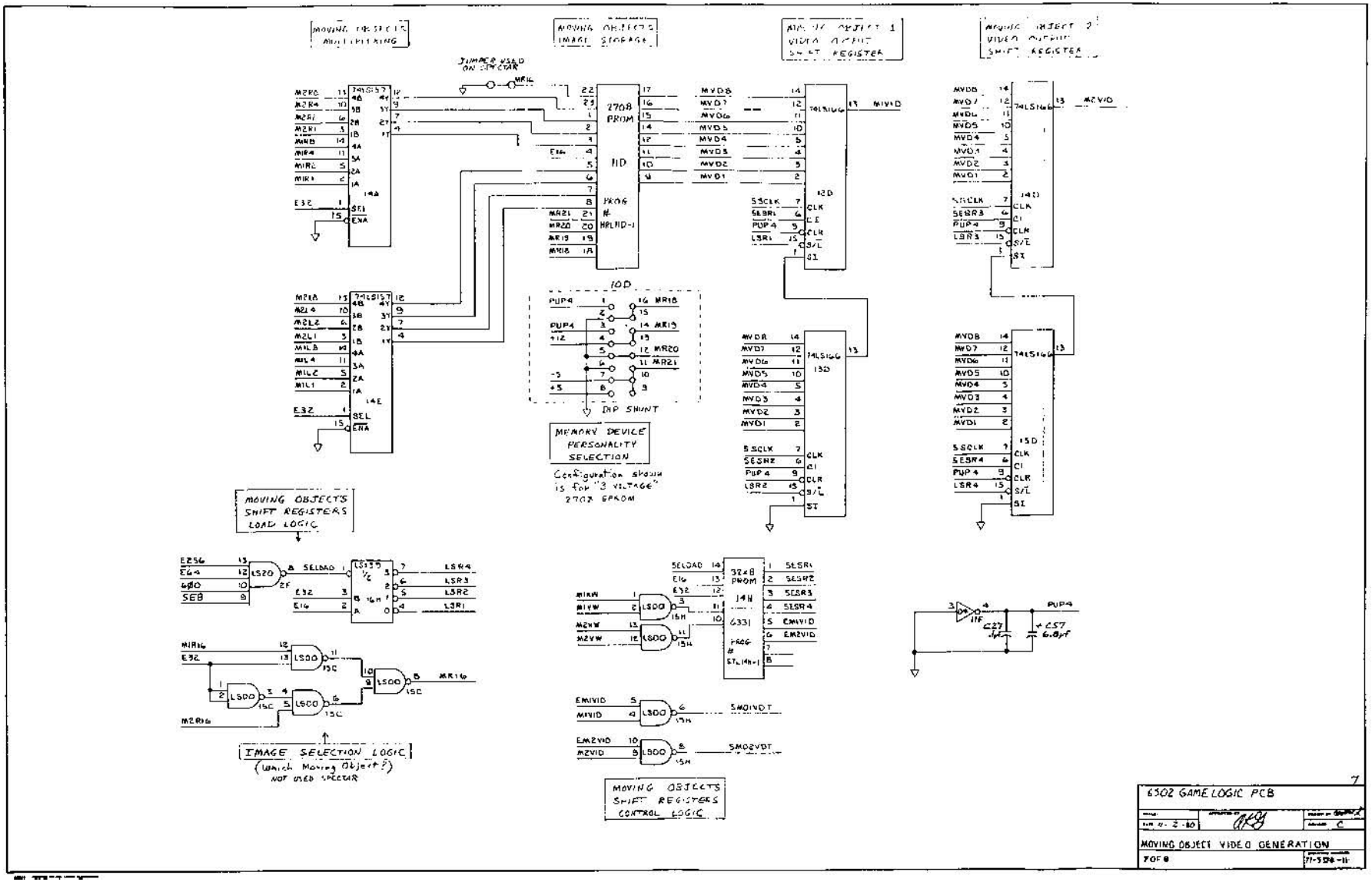
   The lower 2 gates of 15H are, in Spectar, used only for later decoding on the color adapter board.

6. **Memory Device Personality Configuration (10D)**

   This is another Dip Shunt which reconfigures the PC board in order to use a PROM (11D) of another type or manufacturer.

CAUTION

If PROM 11D must be replaced, replace it with the same type if possible. Replacement with a different type PROM without proper reconfiguration of the dip shunt at 10D may cause destruction of the PROM. IF IN DOUBT, CONTACT THE EXIDY SERVICE DEPARTMENT FOR ASSISTANCE.


MOVING OBJECTS IMAGE STORAGE
JUMPER USED ON SPECTAR
2708 PROM
MEMORY DEVICE PERSONALITY SELECTION
Configuration shown is for "3 VOLTAGE" 2708 EPROM
DIP SHUNT
MOVING OBJECTS SHIFT REGISTERS LOAD LOGIC
IMAGE SELECTION LOGIC
(Which Moving Object?)
NOT USED SPECTAR
MOVING OBJECTS SHIFT REGISTERS CONTROL LOGIC
6502 GAME LOGIC PCB
MOVING OBJECT VIDEO GENERATION

GAME LOGIC PCB

1. **Interrupt Status Latch (8E)**

   This latch is set when a coin is dropped or vertical sync occurs. When the latch is set, the CPU is interrupted, that is, signal IRQ goes low. This forces the CPU to jump to the interrupt service routine. The interrupt service routine instructs the CPU to check for a coin input, and then run a debounce routine on the coin bits of ports 9E or 15A, depending on which coin input bit was set at 8E.

   If the CPU finds no coin input bit set at latch 8E, it will assume the Interrupt condition was caused by vertical sync. This tells the CPU that it should now jump to the routine that services the normal game play, and that the screen can now be updated with new data. The screen can only be updated during the vertical retrace interval.

   Note that this latch also has two signals labeled LNG0 and LNG1 which both show PC etched jumpers. These two bits are the select bits for one of four languages, English, French, German, and Spanish. You may select a language by cutting the appropriate jumper, allowing it to be pulled to a logic high. For English, no cutting is necessary. See the Operator's Manual for proper configuration of other languages.

   Also on this latch is the signal named TABLE. This signal, tied to a pullup resistor and switch, determines whether the program operates as a table model or in the upright game configuration. See the Operator's Manual for more details.

2. **Option Switch Port (15A)**

   This port provides input from the option dipswitch, at location 16A. Data from the dipswitch is gated onto the data buss and read by the CPU at game start. This allows such options as number of turns, coins per game, additional game versus extra turn, etc.

   Note that one input of this port (labeled COIN 2) does not come from the switch. Instead, it comes from Coin Input 2, and is used for debouncing the auxiliary coin input switch.

3. **Control Inputs Port (9E)**

   This port provides input from the controls located on the control panel, such as the joystick, fire button, one player start, and two player start. Data from these controls are gated onto the data buss for examination by the CPU during the regular service routine (which is synchronized to the vertical interval).

   Note that one of these inputs is from the COIN1 input (labeled 5COIN1) rather than a game control input. The COIN1 input to this port is used for debouncing the standard coin input.

4. **Moving Image Latch**

   Only the CPU can write to the moving image latch. This latch contains the code that specifies which image or images are presently being displayed by the hardware moving object circuitry.

5. **Audio Board Port**

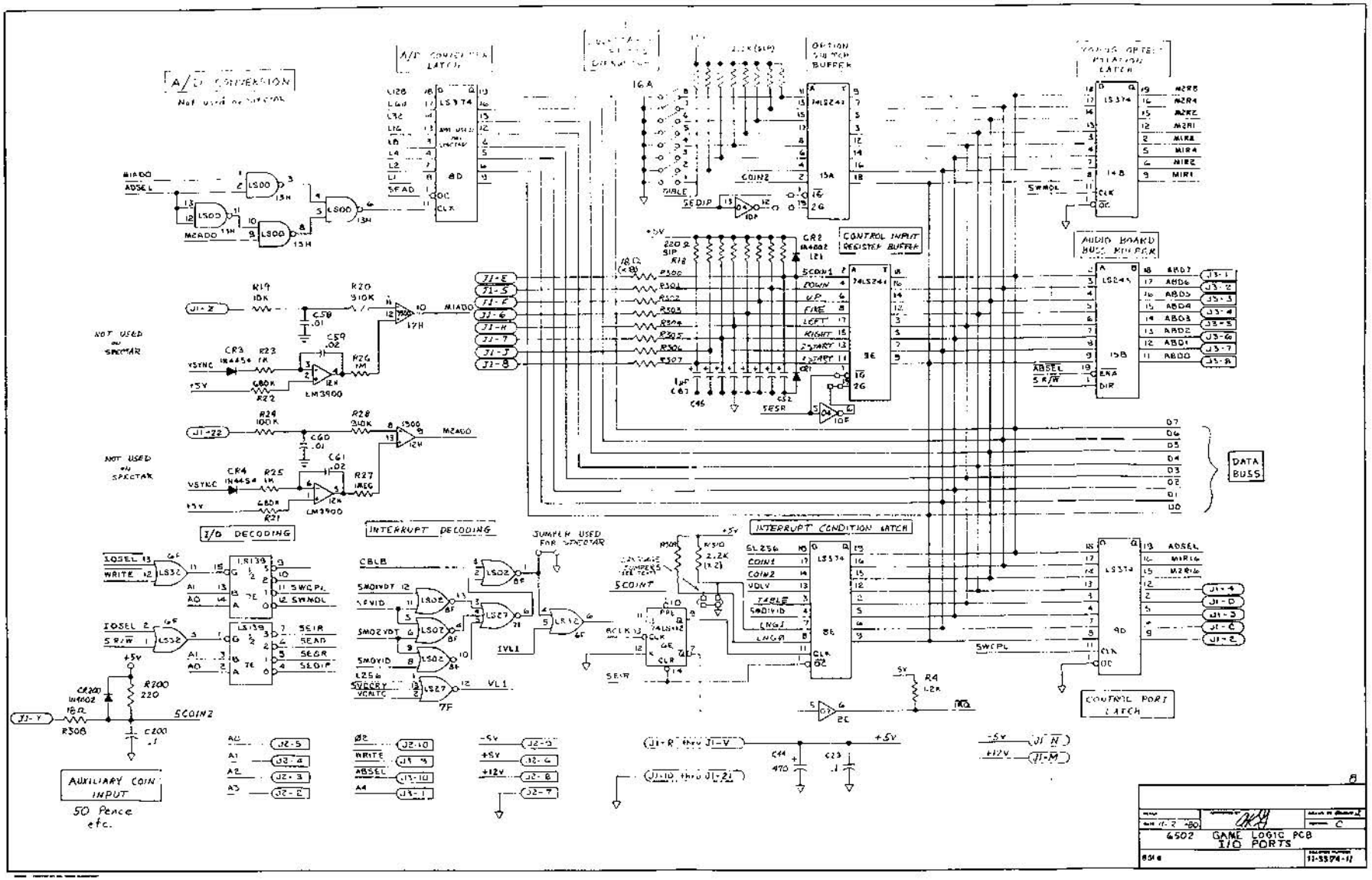
   This latch is written to only by the CPU and transmits instructions to the audio board when any sounds are enabled, disabled, or the game is initialized. For the functions of these instructions, see the audio board schematic and/or description of operation.

6. **Control Port Latch (9D)**

   This latch, used only in the Spectar cocktail table versions, is written to only by the CPU and keeps track of which player is "up", in order to select which controls are active, that is, player one or player two.

7. **I/O Decoding (7E)**

   The upper half of this decoder generates the chip selects for those devices written to by the CPU, and the lower half generates the chip selects for those devices which are read by the CPU. See the detailed memory map for more precise information.


A/D CONVERTER
Not used on Spectar
I/O DECODING
INTERRUPT DECODING
INTERRUPT CONDITION LATCH
CONTROL PORT LATCH
AUDIO BOARD BUSS BUFFER
CONTROL INPUT REGISTER BUFFER
OPTION SW PORT BUFFER
DATA BUSS
AUXILIARY COIN INPUT
50 Pence etc.
6502 GAME LOGIC PCB I/O PORTS
11-5574-11

AUDIO BOARD

1. **Address Decoding (1D)**

   Uses the audio board select signal ABSEL, the 02 AND'ed write signal WRITE, and Address Line A0 to decode the addresses for two input latches. These two latches each receive a byte of data from the CPU instructing the audio board what to do and when.

   Note that address 5200 Hex and 5201 Hex are the intended address, but since only address line A0 is used, these latches respond to even and odd addresses throughout the 52XX Hex region. For example, the latch at 5201 Hex also responds to 5203 Hex, 5217 Hex, and so on, so long as the least significant digit is odd.

2. **Control Data Latch (2C)**

   This latch receives a byte of data from the CPU that sets those particular bits directly used as sound enables. Signal TONE is the enable for the programmable tone (or music) generator. Signal CRASH is the enable for the crash or explosion sound. Signal SHOOT is the enable for the player (Wummel) firing sound. SPECTAR does not use signal CPU MUSIC.

3. **Tone Data Latch (2D)**

   This latch receives a byte of data from the CPU that becomes the preload for the most significant counters of the Tone Generation circuit. Varying this preload allows generation of a variety of tones used for music or special effects.

4. **Tone Generation Circuit (1A, 1B, 3A, 3B, 3D)**

   Counters 1A and 1B divide the 02 (phase two) processor clock down from approximately 706 Khz to approximately 34 Khz. This frequency establishes a range of tones accurately generated by merely changing the preload of the two most significant counters in this circuit, 3A and 3B.

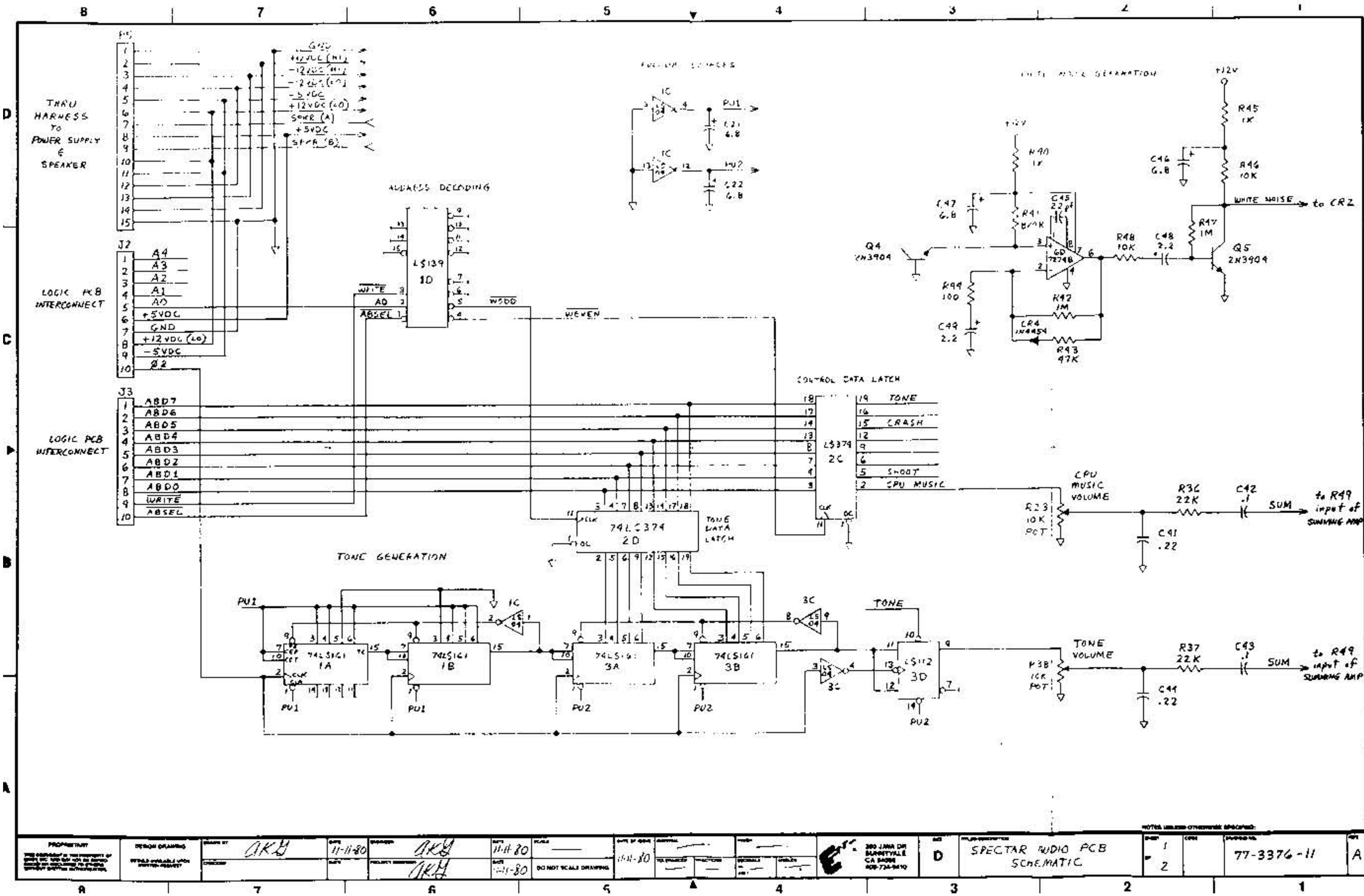
   Flip-flop 3D divides this tone by two again, while transforming a narrow terminal count pulse train into a pulse train having a 50% duty cycle. This means it is at a logic high for the same amount of time it is at a logic low, causing a more pleasing sound to the ear.

   The output of this circuit is then fed to the input of the summing amplifier.

5. **White Noise Generation (6D)**

   Transistor Q4 is the source of this white noise, as its base–emitter junction is broken down by excessive reverse bias. This throws the junction into heavy electron agitation (thermal emission) which activity produces noise across a wide bandwidth.

   Operational Amplifier 6D is used merely to boost the output amplitude of this noise, and transistor Q5 serves as an output buffer stage to prevent loading of the operational amplifier.


THRU HARNESS TO POWER SUPPLY & SPEAKER
LOGIC PCB INTERCONNECT
LOGIC PCB INTERCONNECT
J2
J3
A4
A3
A2
A1
A0
+5VDC
GND
+12VDC (LO)
-5VDC
Ø2
ABD7
ABD6
ABD5
ABD4
ABD3
ABD2
ABD1
ABD0
WRITE
ABSEL
GND
+12VDC (HI)
-12VDC (HI)
-12VDC (LO)
-5VDC
+12VDC (LO)
SPKR (A)
+5VDC
SPKR (B)
ADDRESS DECODING
LS139
1D
WSDD
WEVEN
CONTROL DATA LATCH
LS374
2C
TONE
CRASH
SHOOT
CPU MUSIC
74LS374
2D
TONE DATA LATCH
TONE GENERATION
PU1
PU2
74LS161
1A
1B
3A
3B
3C
1C
LS112
3D
WHITE NOISE to CR2
Q4 2N3904
Q5 2N3904
+12V
R45 1K
R46 10K
R47 1M
C46 6.8
R40 1K
R41 8.2K
C45 22pF
C47 6.8
R48 10K
C48 2.2
R44 100
C49 2.2
R42 1M
CR4 1N4454
R43 47K
CPU MUSIC VOLUME
R23 10K POT
R36 22K
C42 .1
C41 .22
SUM
to R49 input of SUMMING AMP
TONE VOLUME
R38 10K POT
R37 22K
C43 .1
C44 .22
C21 6.8
C22 6.8
SPECTAR AUDIO PCB SCHEMATIC
77-3376-11
D
A
1
2
11-11-80
DO NOT SCALE DRAWING

AUDIO BOARD

1. **Shoot Sound Generation (5A, 4A)**

   Both segments of timer 5A are configured to act as free-running multivibrators. The segment on the right receives, as control voltage input, the psuedo-triangle wave created by the charge and discharge of the RC network of the left segment. This creates, in the right segment, a frequency that increases and decreases at the rate of the triangle wave rate. This effectively simulates reverberation.

   This reverberated tone is then fed to amplitude modulator 4A, whose output amplitude is controlled by the voltage applied to pin 2.

   Normally (in the quiescent condition) transistor Q1 is in a saturated state, holding 4A pin 2 at a level just under 6 volts. This prevents any audible output from 4A. When signal SHOOT is enabled (set high), transistor Q1 is cut off due to the base being dragged low. This drops the voltage on 4A pin 2 low causing the output amplitude of 4A to increase, creating the player firing sound. Note that both the leading and trailing edge of this amplitude-modulated tone package are made gradual (sloping) due to (for the leading edge) the discharge time of C60, and (for the trailing edge) the discharge time of C14.

2. **Explosion/Crash Sound Generation (Q3)**

   Normally (quiescent condition) transistor Q3 is not base-biased to conduct, therefore the white noise applied to the cathode of CR2 is never passed through the circuit. When signal CRASH is enabled (set high), C35 is allowed to charge through CR1 and R25 toward +12v. As this voltage increases, the base of Q3 receives increasing current and begins to pass the white noise.

   This circuit is configured to act as an active filter, so the frequencies passed are only those selected for a reasonable crash or explosion sound.

   The trailing edge of the explosion/crash decays slowly when signal CRASH is disabled (set low) since the discharge path for C35 is through a relatively high resistance (R24).

   Output of this circuit is also then routed to the input of the summing amp.

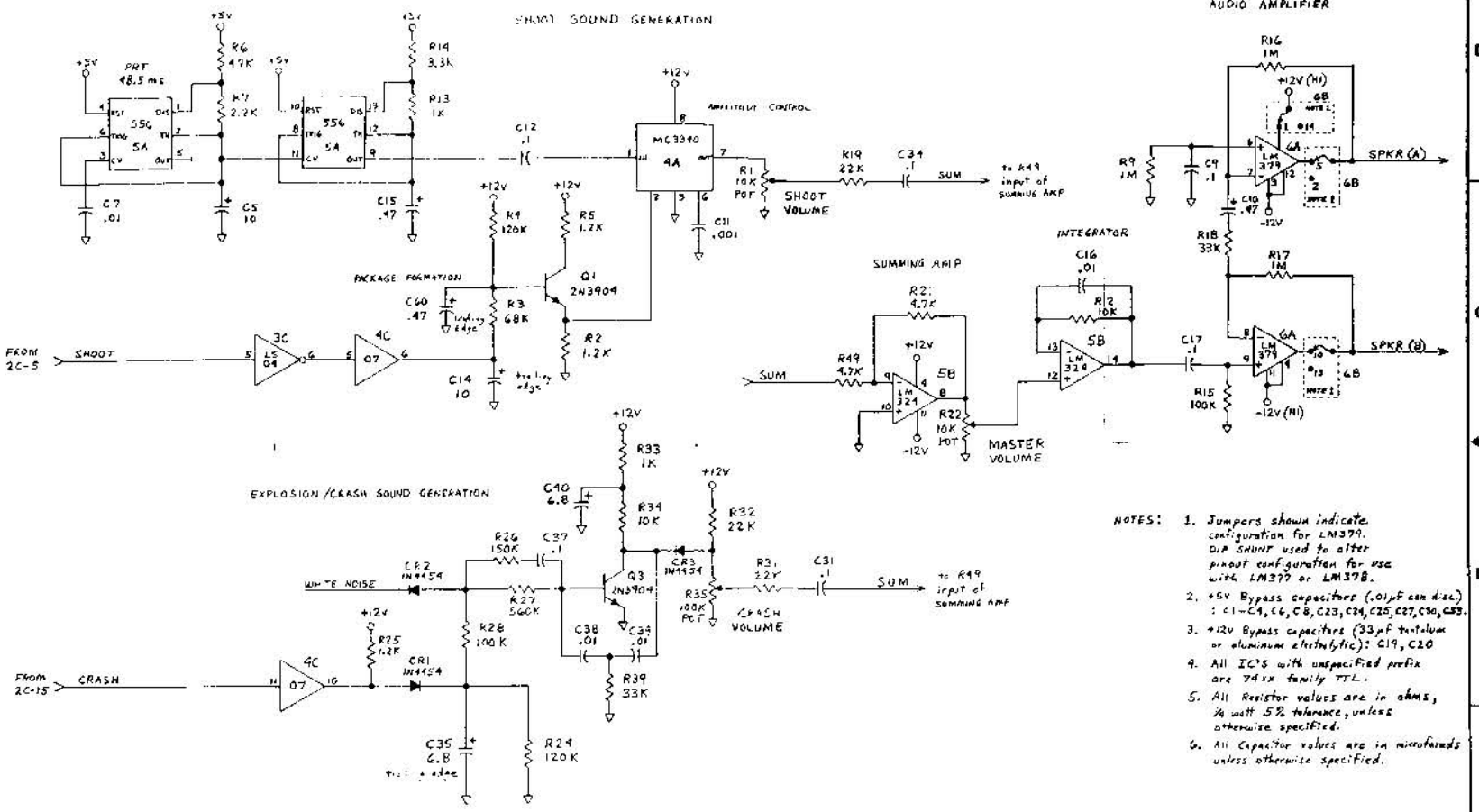
3. **Summing Amplifier and Integrator (5B)**

   Two segments of an LM324 operational amplifier are used here. The first is configured as a summing amplifier. It is the common point at which all the various sounds are algebraically added to become one signal. This signal is the composite of all individually developed sounds. This is also the location of the master volume control (R22).

4. **Audio Amplifier (6A)**

   The final audio amplifer is a single IC (6A), configured as a bridge amplifier. The composite audio signal is applied to the input of one of the two internal segments and the output swings in accordance with the input signal. The feedback on this segment is not only fed back to the inverting input of the same segment, but is also applied to the inverting input of the other segment. This creates a condition wherein one segment swings positive, and the other segment simultaneously swings in a negative direction, creating an output twice the voltage of a single segment.

   Note three types of audio amplifier IC's may be found in this position. All are identical except for the total power output and pinout. They are LM377 DUAL 2W, LM378 Dual 4W, and LM 379 Dual 6W.


SHOOT SOUND GENERATION
AUDIO AMPLIFIER
PRT
48.5 ms
SHOOT VOLUME
SUM
to R49 input of SUMMING AMP
AMPLITUDE CONTROL
PACKAGE FORMATION
FROM 2C-5
SHOOT
SUMMING AMP
INTEGRATOR
MASTER VOLUME
SPKR (A)
SPKR (B)
EXPLOSION /CRASH SOUND GENERATION
WHITE NOISE
CRASH VOLUME
FROM 2C-15
CRASH
NOTES:
1. Jumpers shown indicate configuration for LM379. DIP SHUNT used to alter pinout configuration for use with LM377 or LM378.
2. +5V Bypass capacitors (.01μF can disc) : C1-C4, C6, C8, C23, C24, C25, C27, C30, C33.
3. +12V Bypass capacitors (33μF tantalum or aluminum electrolytic): C19, C20
4. All IC's with unspecified prefix are 74xx family TTL.
5. All Resistor values are in ohms, ¼ watt 5% tolerance, unless otherwise specified.
6. All Capacitor values are in microfarads unless otherwise specified.
D
SPECTAR AUDIO PCB SCHEMATIC
77-3376-11
A

COLOR ADAPTER BOARD

1. **Character Generator RAM Division (1A, 2A)**

   The combination of flip-flop 1A and decoder 2A divides the character generator RAM into 4 equal segments, using the uppermost 2 address lines from that circuit (VD7A09, VD7A10) and the composite video signal (5CV1D).

   The resulting 4 video lines are then applied to the input of the priority encoder at 2B.

2. **Video Prioritization (2B)**

   All video outputs from the Logic Board are applied to priority encoder 2B. As mentioned in the discussion of "Character Generator RAM Division", above, the single character generator output has here been separated into 4 different lines, each carrying the video imagery stored in a different quadrant of character generator RAM. These four lines are applied to the priority encoder along with the video output lines from Moving Object 1, Moving Object 2, and signal 5LINES, not used for SPECTAR.

   As shown on the schematic, the input prioritization is from top to bottom. That is, highest priority is assigned to the input shown at the top (5MO1VID) and the lowest to the input at the bottom. The lowest in this case is actually tied low in order to be always active, which creates the background color.

   The code present on the output of 2B indicates the number of the highest priority video line active at that time. This code is then applied to the Color Multiplexers to select the appropriate RGB output code for that video imagery.

3. **Color Multiplexers (5A, 5B, 5C)**

   Each of these multiplexers generates the final video output for a particular base color: red, green, or blue.

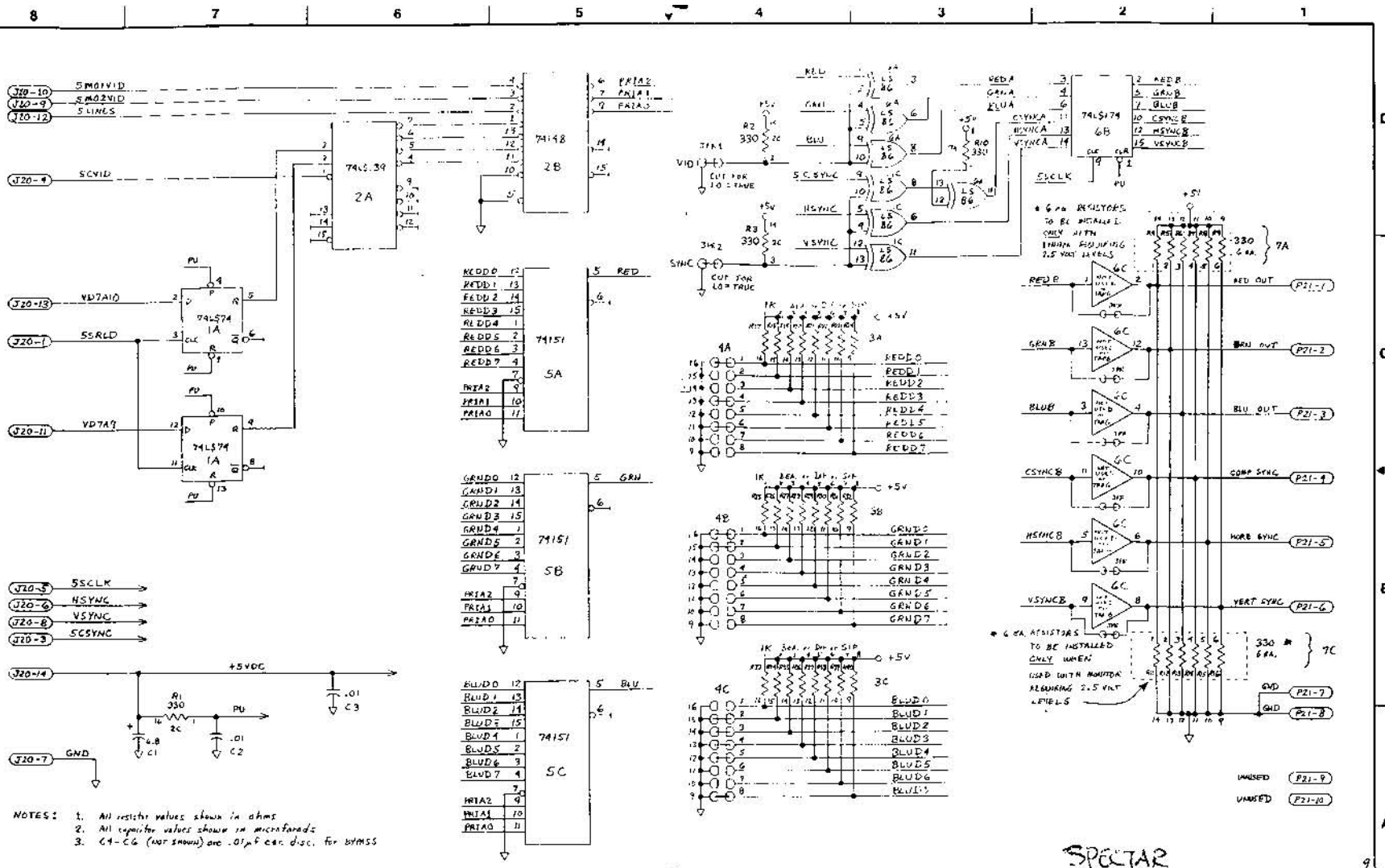
   The priority code from 2B is applied to the multiplexer select lines. This causes all multiplexers to simultaneously output data according to the priority code, and output the data from a particular input pin. The data on each input pin is set up by jumper configuration. Thus, in parallel, 5A, 5B, and 5C consider two factors when outputting RED, GREEN and BLUE data: the code of the highest priority video present, and the associated jumper configuration establishing the color of the video.

4. **SYNC and VIDEO Polarity (JPR1, JPR2)**

   Exclusive OR gates 6A and 1C have here been configured to act as "selectable inverters". Cut the VID jumper (JPR1) and the output video is inverted to become negative true. The same occurs with the SYNC jumper (JPR2). Note that composite sync is available as well as separate Horizontal and Vertical sync outputs. When JPR2 is cut, it inverts all three sync outputs.

5. **Output Level Adjustments (6C, 7A, 7C)**

   The only time these inputs are used is with a monitor requiring unusual input levels. They are not used on SPECTAR.


J20-10 5MOIVID
J20-9 5MO2VID
J20-12 5 LINES
J20-4 SCVID
J20-13 VD7A10
J20-1 5SRLD
J20-11 VD7A9
J20-5 5SCLK
J20-6 HSYNC
J20-8 VSYNC
J20-3 5CSYNC
J20-14 +5VDC
J20-7 GND
74LS139 2A
74148 2B
74LS74 1A
74LS74 1A
74151 5A
74151 5B
74151 5C
R1 330 2C
C1 6.8
C2 .01
C3 .01
R2 330 1C
R3 330 2C
R10 330 1A
VID1
SYNC
CUT FOR LO=TRUE
5 C. SYNC
HSYNC
VSYNC
74LS174 6B
5SCLK
1K 4EA. +5V
3A
4A
3B
4B
3C
4C
330 6 EA. 7A
330 6 EA. 7C
RED OUT P21-1
GRN OUT P21-2
BLU OUT P21-3
COMP SYNC P21-4
HORZ SYNC P21-5
VERT SYNC P21-6
GND P21-7
GND P21-8
UNUSED P21-9
UNUSED P21-10
* 6 EA. RESISTORS TO BE INSTALLED ONLY WHEN USED WITH MONITOR REQUIRING 2.5 VOLT LEVELS
NOTES: 1. All resistor values shown in ohms
2. All capacitor values shown in microfarads
3. C4-C6 (not shown) are .01μF cer. disc. for BYMSS
SPECTAR
6502 Based VIDEO GAME
COLOR ADAPTER PCB
77-3373-11
D
B
1-24-80
4-24-80
1 OF 1

APPENDIX A

PARTS LIST FOR SPECTAR

Control Panel Assembly

Part Number	Description
68-2033-13	control panel
75-5177-10	control panel PSA polycarb silkscreen overlay
72-3022	switch pushbutton with nut and washer
38-5076-10	control 4-way joysick, long assy.
38-5044-10	Midway white pushbutton switch assy.
74-5247	carriage bolts 10/24 x 5/8 L black full thread
74-6506	kepnut 10/24
71-2391	control panel harness

Universal Power Supply Assy

Part Number	Description
78-3001	+5VDC Power Supply 6AMP
63-4028	aux. transformer T911
or	
63-4025	aux. transformer T893
or	
63-4035	MFG pin 773P9
77-3365-15	power supply PCB Assy.
71-2389-10	power supply harness
76-1211-10	power supply mounting board
74-3503	screw, #6x1/2 l phillips pan head selftap
74-5198	screw, #6-32x 3/4 pan hol. phil. machine
74-3502	kepnut 6-32
74-3500	washer #6 Amer. std plain
74-4604	hex nut 8-32 nylon
61-8072	butt splice, blue
61-8056	plug, 2 pin molex
61-8054	pins, male molex
88-4002	tie wrap, small
88-4001	tie wrap, large
88-4028	wire, 22 ga. buss-uncoated
88-4008	solder SN60 .03 dia. 58 core
88-4011	flex mask and mold seal

American Standard Double Coin Door

Part Number	Description
66-4003	Std. double coindoor, Vendall
66-4007	25 cent Amer. coin acceptor
	Coin door key (supplied w/ 66-4003)
71-2390	Universal coin door harness
64-2000	coin meter
88-4002	tie wrap, small
61-8313	butt splice red
74-3502	6-32 kepnut

British/Australian Coin Door

Part Number	Description
66-4013-10	Std. British/Aust. dbl. coindoor w/ 10P/50P Coin door key supplied w/ 66-4013-10
71-2417	Aux. coin harness
64-2000	coin meter
61-8313	butt splice red
71-2390	univ. coin door harness
74-3502	6-32 kepnuts

Pushbutton Assy

Part Number	Description
72-3061	switch assy.
72-3062	push button
74-0203	pal nut

Spectar Speaker Assy

Part Number	Description	Reference Location
62-7061	6" x 9" oval speaker	
61-8056	conn. 2 pin male molex 03-09-2022	P4
61-8054	pins, male molex 02-09-2118	

Monitor Isolation Transformer Assy.

Part Number	Description	Reference Location
FR 63-4029	Isolation transformer Midwest 773P7	
61-8058	Molex connector 03-09-2032	AC INPUT 22
61-8054	male molex pins 02-09-2118	P22
61-8057	molex connector 03-09-1023	AC to Monitor J23
61-8055	female molex pins 02-09-1118	J23
76-1212-50	XFMR mounting board	
71-2001-14	xfmr harness	
61-8072	butt splice blue	
74-6402	washer, #10 plain	
74-6506	kepnut 10-24	
74-5463-01	screw, 10-24 x 1" ph phil mach	
74-5165	fender washer 1/4 ID 1 1/4 OD	
88-4002	tie wrap small	
61-8313	butt splice red	

Audio PCB Assembly

Part Number	Description	Reference Location
48-2321	74LS139, IC	1D
48-2314	74LS374, IC	2C,2D
48-2071	74LS112, IC	3D
48-2308	74LS161, IC	1A,2A,1B,3B, 3A
48-2210	72748, IC	6D
48-2342	LM324	5B
48-2212	NE 556	5A
48-2221	MC 3340	4A
48-2211	LM379 (Dual 6W Audio Amp National)	6A
48-2015	7407	4C
48-2302	74 LS04	1C,3C
47-3005	2N 3904, trans	Q1,Q3,Q4,Q5
46-3030	IN 4454, trans	CR2, CR3, CR4, CR1
59-5110	resistor, 2.2K 1/4 w 5%	R7
59-5100	resistor, 3.3K 1/4 w 5%	R14
54-5021	potentiometer, 100K	R35
54-5019	potentiometer, 10K	R1,R22,R38
59-5070	resistor, 22K 1/4w 5%	R19,R31,R32, R37
59-5125	resistor, 1K 1/4w 5%	R33,R40,R45, R13
59-5163	resistor 820K 1/4w 5%	R41
59-5025	resistor 1 meg omega 1/4 w 5%	R9,R16,R17, R42, R47
59-5055	resistor, 47K 1/4 w 5%	R43
59-5080	resistor, 10K 1/4 w 5%	R12,R34,R46 R48
59-5140	resistor, 100K omega 1/4w 5%	R44
59-5069	resistor, 120K 1/4w 5%	R4, R24
59-5050	resistor, 68K 1/4w 5%	R3
59-5120	resistor, 1.2K 1/4w 5%	R2,R25,R5
59-5095	resistor, 4.7K 1/4w 5%	R21, R49, R6
59-5045	resistor, 100K 1/4w 5%	R28, R15
59-5040	resistor, 150K 1/4w 5%	R26
59-5030	resistor, 560K 1/4w 5%	R27
59-5065	resistor, 33K 1/4w 5%	R18, R39
23-4030	cap, .22 uf ceramic disk	C44
23-4035	cap .1 uf ceramic disk	C9, C12, C17, C31, C34, C37, C43
23-4015	cap, 6.8 uf 25v dip. tant.	C14, C21, C22, C40, C46, C47
21-4020	cap, 2.2 uf 15v dip. tant.	C48, C49
23-4070	cap, 22pf. ceramic disk	C45

Audio PCB Assembly (continued)

Part Number	Description	Reference Location
23-4060	cap, .001 uf ceramic disk	C11
23-4050	cap, .01 uf ceramic disk	C1, C2, C3, C4, C6, C7, C8, C16, C24, C25, C27, C28, C30, C33, C38, C39
21-4010	cap, 33 uf 25v dip tant.	C19, C20
22-4025	cap, .47 uf 25v dip. tat.	C15, C10, C60
61-8042	conn., 10 pin female	J2, J3
68-3041	heat sink, thermalloy 6072	6A (use only w/ LM 379
22-4032	caps, 10 uf Radial tant or mini electro 25V	C14, C5
74-2506	screw, 4-40 x 1/4" machine	6A heatsink
72-3025	dip pkg. shunt 16 pin AMP Part # 435704-8	6B
74-5065 or	standoff 6-32 x 5/8" nylon	
74-5075	standoff 6-32 x 1/2" nylon	
77-3371	Spectar, audio (bare) PCB	
74-5182	6-32 x 1/4 machine screw	

Universal Power Supply PCB

Part Number	Description
77-3365-14	printed circuit board
20-4000	4000 uf 50 v axial lead capacitor
21-4010	33 uf 25 v dip tantalum capacitor
21-4015	6.8 uf 35v dip tantalum capacitor
46-3016	60si diode
47-3004	mda 970-1 bridge rectifier
47-3041	"N3055 transistor
47-3011	2N6246 transistor
48-2337	7905T negative 5v LM320T-5 regulator
48-2217	7912T negative 12v LM320T 12 regulator
48-2338	7812T positive 12v LM340 T-12 regulator
68-3041	thermalloy 6072 heat sink
69-2038	thermalloy 6015 heat sink
61-8010	12 pin male molex
74-2514	4-40 x 3/8 phillips pan head machine screw
74-5216	#4 flat metal washer
74-5191	#4-40 kep nut

6502 Game Logic PCB Assembly

Part Number	Description	Reference Location
48-2000	IC 7400	3D, 15H
48-2005	IC 7402	1H, 6H
48-2010	IC 7404	1D, 3F, 4D, 10F, 11F
48-2015	IC 7407	2C
48-2020	IC 7408	5E
48-2332	IC 74LS11	3H
48-2035	IC 7420	2F
48-2316	IC 74LS21	12F, 15E
48-2045	IC 7427	7F, 2H
48-2055	IC 7432	6F
48-2067	IC 7474	1C
48-2071	IC 74LS112	2E, 6E
48-2307	IC 74LS138	5B, 5D
48-2321	IC 74LS139	7E, 16H
48-2090	IC 74157	14A, 14E
48-2095	IC 74161	1E,2D,4F,5F
48-2100	IC 74166	12B, 12D, 13D, 14D, 15D
48-2115	IC 74193	10E, 12E, 13F, 15F 14F, 16F, 11E,13E
48-2328	IC, 74LS241	8C, 1A, 3A 3B, 4H, 6B, 7D, 9B, 9E, 15A
48-2350	IC 74LS245	3C, 4C, 6C 15B, 13B
48-2314	IC 74LS374	1F, 14B, 7C, 8E
48-6502	microprocessor 6502	2A
48-2334	2114 (1K x4) RAM	4A, 5A, 7B, 8B, 11C, 12C 13C, 14C
48-9125-01	2708 EPROM (1K x 8) HRL 11D-1	11D
48-9099-01	6331 PROM (.32 X 8)	6D
48-9099-02	6331 PROM (.32 X 8)	14H
48-9144	6301 PROM (256 X 4)	5C
46-3025	IN4002 diodes	8E, 9E, 2H
59-5135	res. 470 omega 1/4 w 5%	1D, 2H
59-5120	res., 1.2K 1/4w 5%	2C
59-5115	res., 1.8K 1/4w 5%	1C, 2C
59-5110	res., 2.2K 1/4w 5%	7E, 2A
59-5105	res., 2.7K 1/4W 5%	1C, 2C
51-0003	res., 220 omega 1/4w 5% 10 pin sip	9E
51-0002	res., 2.2K 1/4w 5% 10 pin sip	16A
51-0001	res., 4.7K 1/4w 5% 10 pin sip	15A

6502 Game Logic PCB Assembly (continued)

Part Number	Description	Reference Location
51-0004	res., 6.8K 1/4w 5% 10 pin sip	14A
23-4033	cap, .01 uf ceramic disc	1D
23-4035	cap, .1 uf ceramic disc	A/R per assy drawing
21-4015	cap, 6.8 uf 25v tant. dip	1C, 6E, 15D, 13F
20-4014	cap, 33 uf 25v electrolytic	IC 2C
20-4005	cap, 470 uf 10v electrolytic	10H
72-3025	dip shunt jumper paks 16 pin	4B, 10D, 11B
72-3042	dip switch 8 pos.	16A
45-3036	crystal, 11.289	1D
61-8041	connector 10 pin molex	16C, 16E
61-8062	dip sockets 16 pin low profile	5C, 6D, 14H
77-3374	print. circuit board	
61-8045	dip socket 24 pin low profile	11D,6A,7A,8A 9A, 10A, 11A
61-8035	dip socket 40 pin low profile	2A
61-8060	dip socket 14 pin low profile	16B
61-8157	dip socket 18 pin low profile	4A 5A 7B 8B 11C 12C 13C 14C
21-4021	cap, 1 uf 25V dip tant	C45, C52
49-5138	res, 220 v 1/4 w 5%	R200, R311 at 5D
59-5064	res, 18ohm 1/4w 5%	R300-R308
23-4067	cap, 330 pf cer. disk	5D
48-9143-01	2716 EPROM programmed SPL6A-1	
48-9143-02	2716 EPROM programmed SPL7A-1	
48-0143-03	2716 EPROM programmed SPL8A-1	
48-9143-04	2716 EPROM programmed SPLA9A-1	
48-9143-05	2716 EPROM programmed SPL10A-1	
48-9143-06	2716 EPROM programmed SPL11A-1	

6502 Color Adapter PCB Assembly

Part Number	Description	Reference Location
48-2080	IC 74151	5A, 5B, 5C
48-2305	IC 74LS74	1A
48-2321	IC 74LS139	2A
48-2079	IC 74148	2B
48-2341	IC 74LS86	IC 6A
48-2333	IC 74LS174	6B
20-4015	6.8 uf dipped tantalum capacitor	C1
59-5136	resistor 330 omega 1/4 w 5%	R1 thru R10
59-5103	9 pin sip resistor pac 1K omega	3A, 3B, 3C
23-4033	.01 uf ceramic disc capacitor	C2 C4 C5 C6
61-8203	10 pin male molex connector	P2
61-8127	14 pin socket stan profile w/ lock	J1
77-3373-14	printed circuit board	